HELMHOLTZ ZENTRUM BERLIN
für Materialien und Energie

Bericht der Herbsttagung der

Studiengruppe für Elektronische Instrumentierung

22. – 24. September 2008

Max-Planck-Institut für Plasmaphysik, Teilinstitut Greifswald, IPP

Herausgeber: Dr. F. Wulf

HMI-B 623 Berlin, Dezember 2008

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Teilnehmer der SEI-Herbsttagung 2008, Max-Planck-Institut, IPP Greifswald

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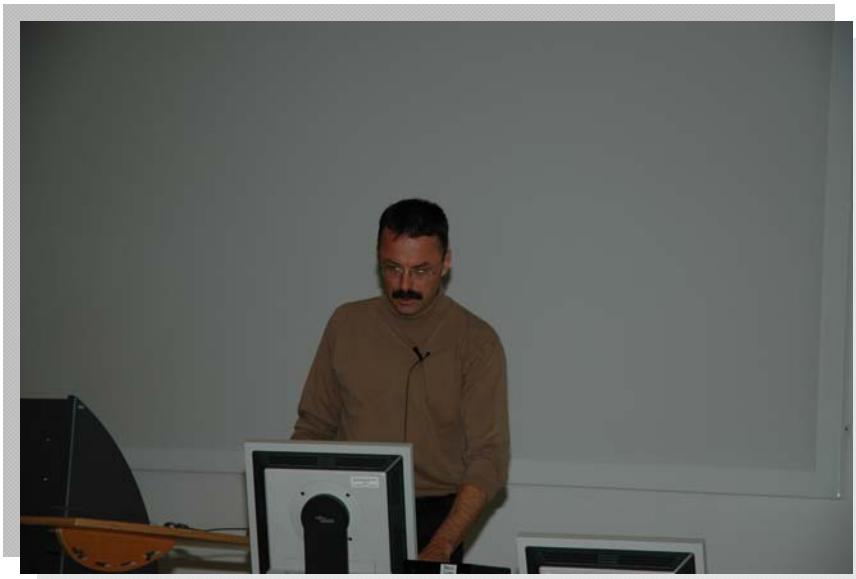
Dr. Friedrich Wulf, Helmholtz-Zentrum Berlin



Prof. Dr. Robert Wolf, Max-Planck-Institut, IPP Greifswald

Dr. Klaus Petry, FZ Karlsruhe

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Vorträge

Dr. Holger Brand, GSI Darmstadt

Dr. Sven Bönisch, Helmholtz-Zentrum Berlin

Kolloqium

HELMHOLTZ ZENTRUM BERLIN für Materialien und Energie

Zusammenfassung

Dr.-Ing. F. Wulf

Die 97. Tagung der **S**tudiengruppe für **e**lektronische **I**nstrumentierung (SEI-Herbsttagung 2008) fand vom 22. bis 24. September 2008 im Max-Planck-Insititut für Plasmaphysik (IPP) - Teilinstitut Greifswald - statt. Der Tagungsband enthält 14 Beiträge aus den unterschiedlichen Bereichen der Informationstechnik und der Steuerungstechnik für Großgeräte, insbesondere Wendelstein 7-X. Ich danke allen Vortragenden und Autoren für die sehr interessanten Beiträge. Mein besonderer Dank gilt Herrn Prof. Dr. R. Wolf und seinen Mitarbeitern für die gute Organisation und informative Besichtigung des Aufbaus von Wendelstein 7-X. Die Beteiligung mit 41 Personen aus 21 Forschungseinrichtungen und Industriefirmen ermöglichte wieder eine intensive Diskussion über die Instrumentierung komplexer Experimentsysteme und Großanlagen.

Der Stellarator Wendelstein 7-X ist ein ehrgeiziges Projekt und ein wichtiger Baustein für die Entwicklung zukünftiger Fusionsreaktoren. Die Inbetriebnahme soll 2014 erfolgen und das erste Plasma (8 MW 10 s Entladung) erwartet man Anfang 2015. Die volle Ausbaustufe mit 10 MW Dauerbetrieb wird für 2019/20 angestrebt. Das Kontrollsystem ist eine Eigenentwicklung, das für das Projekt WEGA (Wendelstein Experiment in Greifswald zur Ausbildung) entwickelt wurde und als Middleware OPC Technik eingesetzt wird. Für die schnelle Datenerfassung wurde ein Konzept für eine serielle Übertragung der Daten mit einer Bandbreite von 700 MB/s und einer zeitlichen Korrelation von 20 ns entwickelt. Die Quenchdetektion für Wendelstein 7-X wurde zusammen mit dem Institut für Prozessdatenverarbeitung und Elektronik (IPE) des Karlsruher Institut für Technologie (KIT) entwickelt. Es ist ausgelegt für 600 Detektoren, nutzt QVersion, LabVIEW, ADWin Komponenten und besitzt eine Schnittstelle zu WinCC. Das System ist auch für ITER einsetzbar und das KIT nimmt deshalb auch an der Ausschreibung für die Instrumentierung von ITER teil.

Die Weiterentwicklung der LabVIEW Plattform ermöglicht deren Einsatz auch für große Steuerungs- und DAQ-Systeme. Auf der unteren Ebene wird das erweiterte CompactRio System direkt mit EPICS verbunden und ermöglicht ein einfaches Plug and Play. Objektorientierte Konzepte wurden in LabVIEW mit der Version 8.2 (LVOOP) eingeführt. Im Gegensatz zu konventionellen Programmiersprachen, wie C^{++} oder JAVA, folgt LabVIEW dem Datenfluss-Paradigma. Das gilt auch für LVOOP. LabVIEW behandelt Objekte nicht als Entitäten, sondern definiert mit Hilfe der LabVIEW Klassen neue Datentypen. Herr Dr. H. Brand[1] von der GSI hat einen Entwurf für eine Klassenbibliothek erstellt. An der Erstellung und deren Nutzung können sich alle Interessenten beteiligen[2].

Ein weiterer Schwerpunkt der Tagung beschäftigte sich mit dem Einsatz von FPGA für die unterschiedlichen Aufgaben der DAQ und Steuerungstechnik. Hierzu wurden Vorträge über die aktuellen Entwicklungen der Firmen XLINX und Altera gehalten. Der Einsatz in den Forschungseinrichtungen wird erschwert durch die mangelnde Personalkapazität und die kurzfristigen Zeitverträge. Es soll daher versucht werden, die Ressourcen der einzelnen Institute noch stärker zu bündeln. Dafür wurde eine webbasierte Plattform[3] eingerichtet, die

[1] H.Brand@gsi.de

[2] http://wiki.gsi.de/cgi-bin/view/NIUser/LabVIEWObjectOrientedProgramming
http://wiki.gsi.de/cgi-bin/view/NIUser/HGFBaseClassLibrary.

[3] http://wiki.gsi.de/cgi-bin/view/SEI.

eine verstärkte Zusammenarbeit zwischen den Instituten ermöglichen soll. Es wird außerdem angestrebt, eine Vereinbarung mit den Herstellerfirmen zu treffen, die eine kostengünstige Nutzung der FPGA tools und Bibliotheken erlaubt. Ansprechpartner ist Herr P. Kämmerling[4] vom Zentralinstitut für Elektronik (ZEL) im Forschungszentrum Jülich (FZJ).

Die von dem Physikalischen Institut der Universität Heidelberg[5] entwickelte programmierbare LogicBox ist erweitert und für den kommerziellen Vertrieb durch die Firma Plein&Baus GmbH (WIENER) optimiert worden. Die 27 Sub-Board-Typen können einfach zusammengeschaltet und für die entsprechende Anwendung mit LabVIEW programmiert werden. Sie können sowohl in NIM wie auch VME Modulen eingesetzt werden.

Die Entwicklung auf dem Gebiet der LI-Ionen Akkus macht beachtliche Fortschritte. Sie erreichen Leistungsdichten von 4000 W/kg und sollen eine Lebensdauer von mehr als 20 Jahren besitzen.

In einem anschaulichen Bericht wurde über den Start, die Zielsetzung und die technologischen Herausforderungen des Large Hardron Collider LHC berichtet. Alleine die erwartete Datenmenge von 15 PByte (10^{15}) pro Jahr füllt 3 Millionen DVDs, die aufeinander gestapelt so hoch sind wie der Mont Blanc (4800 m).

Für die Messung der transienten Oberflächenphotospannungen von CdS Schichten zur Bestimmung der Relaxationsmechanismen in sehr dünnen Schichten (2-20 nm) wurde im HZB-Berlin ein Messsystem mit sehr hochohmigen (10 GΩ, C_{in}< 1pF) differenziellen Eingängen entwickelt. Es ermöglicht erstmals die Messungen über einen Zeitbereich von 10 ns bis 0,1 s mit einer Auflösung von 14 Bit, 100MS/s, die für einen Transienten 10^8 Datenpunkte aufnimmt.

Voraussetzung für derartige Entwicklungen sind leistungsfähige und moderne Messgeräte, die auf der Industrieausstellung vorgestellt wurden. Ergänzt wurden die Informationen durch den Vortrag der Firma Rohde & Schwarz über die Messung von Phasenrauschen und dem Bericht über die neue Oszillografen Generation der Firma LeCroy, die u.a. über einen sehr schnellen Datentransfer verfügen.

Die SEI-Frühjahrstagung 2009 findet vom 23. bis 25. März 2009 im Zentralinstitut für Elektronik (ZEL) im Forschungszentrum Jülich statt. Die SEI-Herbsttagung ist vom 21. bis 23. September im neuen Helmholtz Zentrum Berlin für Materialien und Energie GmbH geplant.

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[5] vwalter@physi.uni-heidelberg.de

Max-Planck-Institut
für Plasmaphysik

Wendelstein 7-X

Robert Wolf

Max-Planck-Institut für Plasmaphysik, Greifswald

robert.wolf@ipp.mpg.de

Contents

- **Nuclear fusion and magnetic confinement**
- **Magnetic confinement concepts and the role of Wendelstein 7-X**
- **Wendelstein 7-X design and construction**

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Nuclear fusion

Nuclear fusion between deuterium and tritium

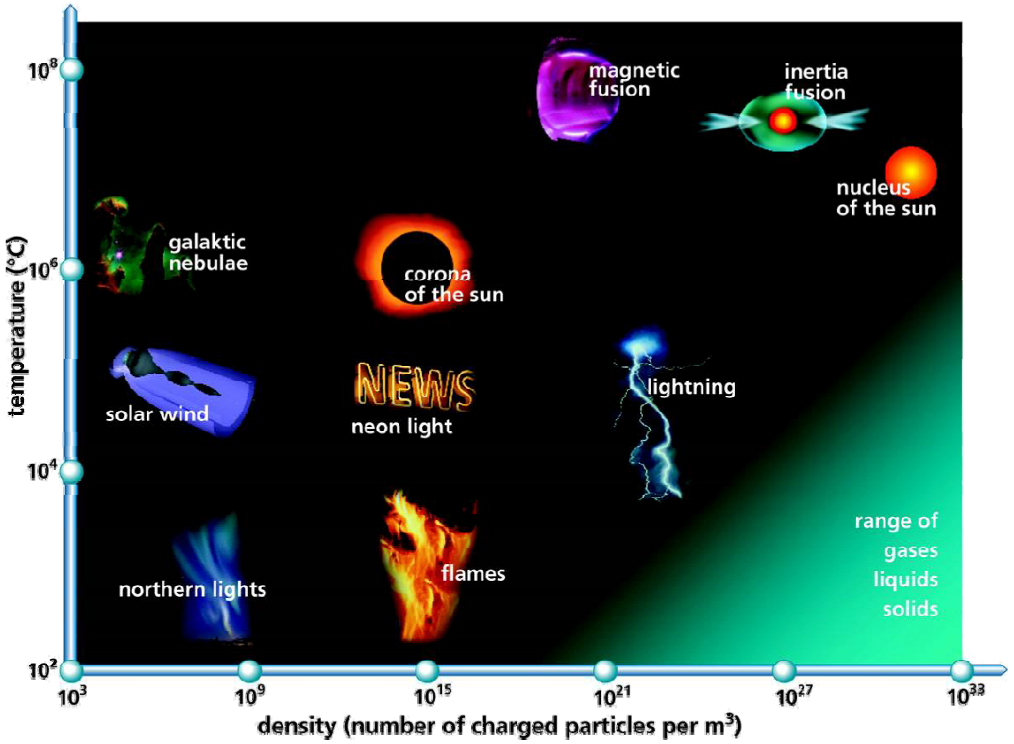
$^{2}D + {}^{3}T \rightarrow {}^{4}He + n + 17{,}6\ MeV$

Tritium has to be bred from Lithium

$n + {}^{6}Li \rightarrow {}^{4}He + {}^{3}T$

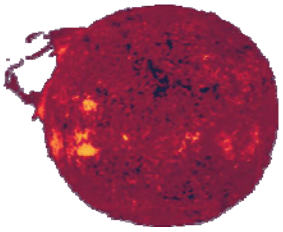
- Fuel for at least one million years (based on today's energy consumption)
- Even distribution of fuel worldwide
- No CO_2 production
- No chain reaction (unlike fission, where the energy of several years is stored in the fuel rods)
- Limited radioactivity (from neutron activation of structural materials)

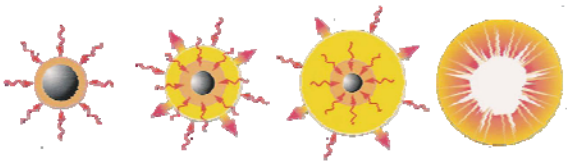
Positive power (energy) balance requires thermal plasma



Confinement of hot fusion plasmas

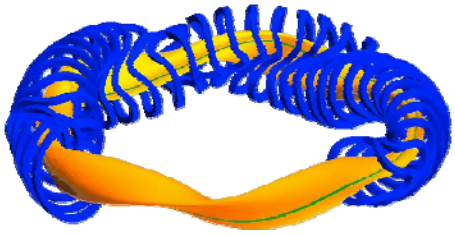
Gravitation
(sun)





Mass inertia (Inertial confinement fusion, hydrogen bomb)

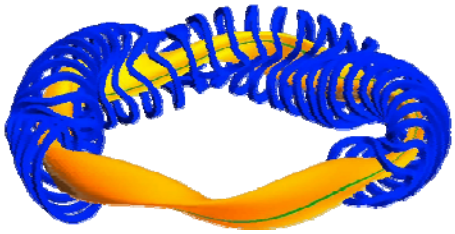
Magnetic fields



Confinement of hot fusion plasmas

- **Temperature > 100 Mio. °C (> 10 keV)**
- **„high" density about 1/500.000 of the atmospheric density (10^{20} m^{-3})**
- **Good thermal insulation energy confinement τ_E > 5 sec**
- **corresponds to 2 atmospheres**

Magnetic fields



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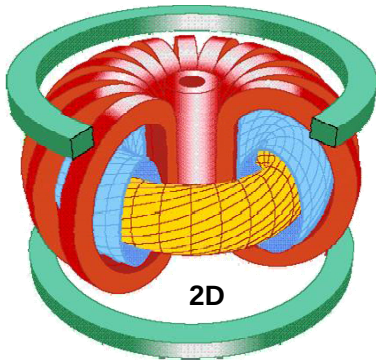
Two magnetic confinement concepts

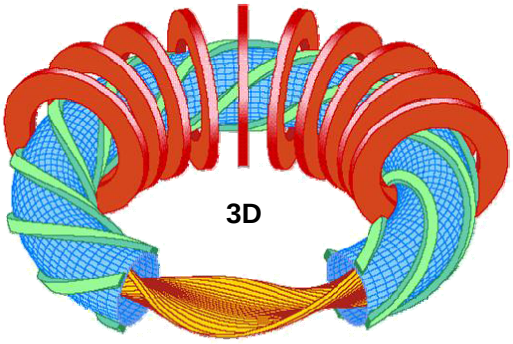
Tokamak



Major part of the magnetic field is generated by strong plasma current

- **Favourable confinement properties**
- **Further developed concept**
- **Pulsed operation**
- **Current driven instabilities / disruptions**

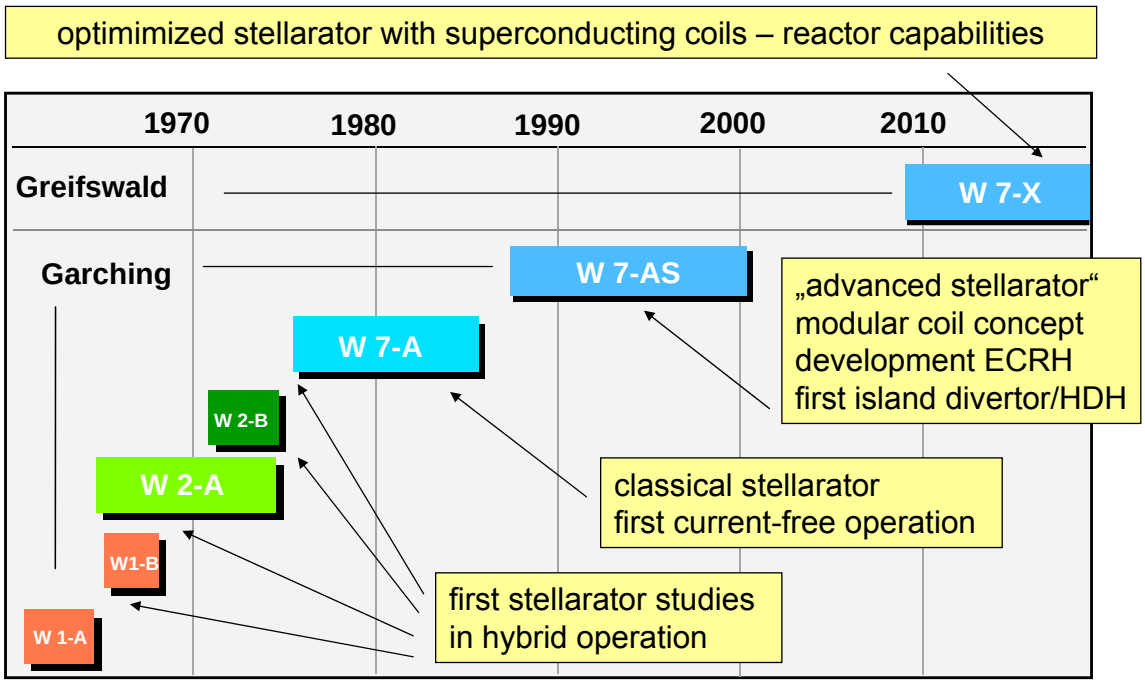
Stellarator



Magnetic field essentially generated by external magnetic field coils

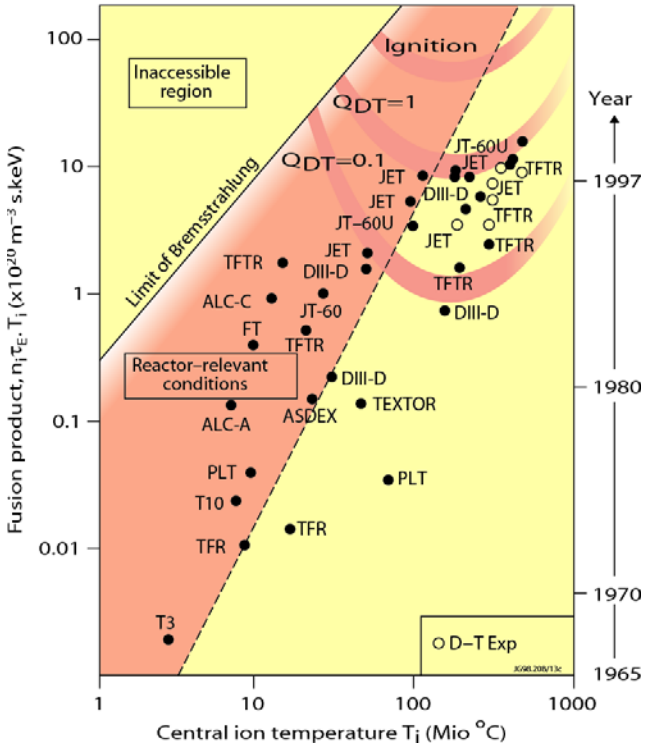
- **Requires elaborate optimization by high performance computers to achieve necessary confinement**
- **Intrinsically steady state**
- **Quiescent operation / soft operational boundaries**

Despite initial set-backs long history of stellarators at IPP



What has been achieved in fusion research

- Doubling of fusion product every 1,8 years
- Up to 400 Mio ºC
- 16 MW of fusion power (for ~ 1 sec)
- …



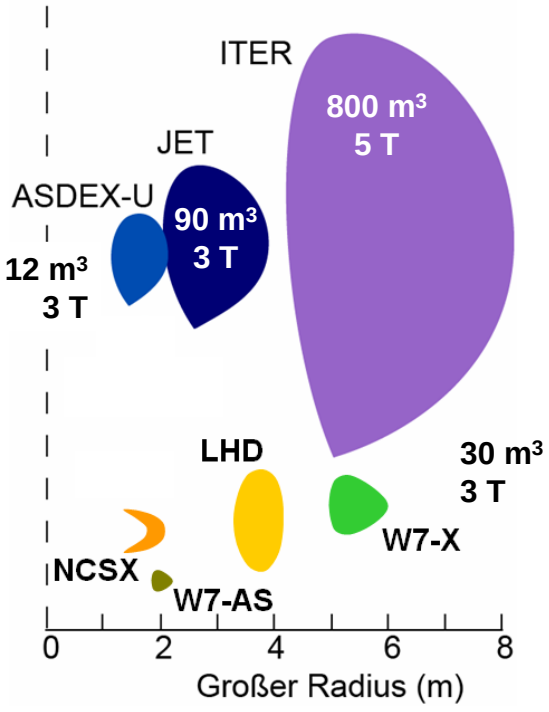
The role of Wendelstein 7-X

ITER (tokamak)

- demonstrate burning fusion plasma (500 MW fusion power, Q = 10)
- scientific and technical basis for demonstration power plant

Wendelstein 7-X

- demonstrate reactor feasibility of stellarator concept
- confinement of fast ions
- plasma exhaust
- steady state operation (10 MW plasmas for 30 minutes)



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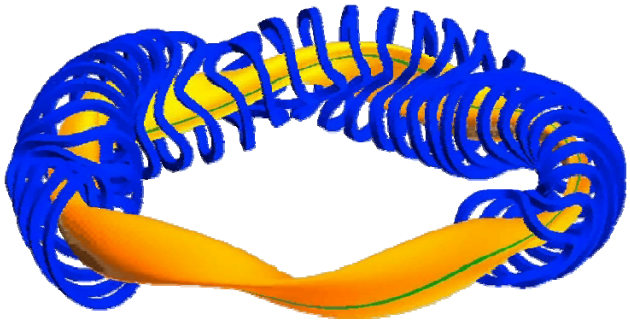
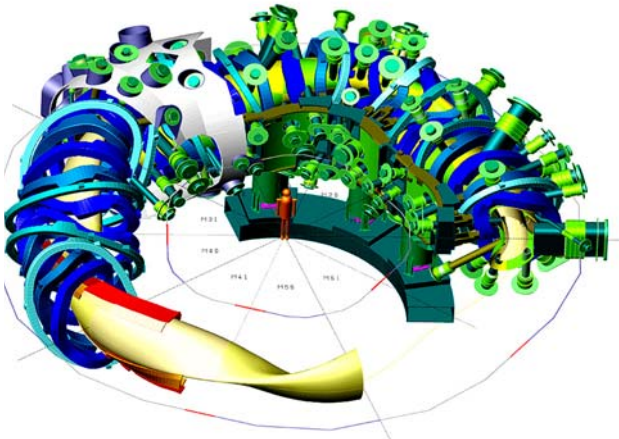
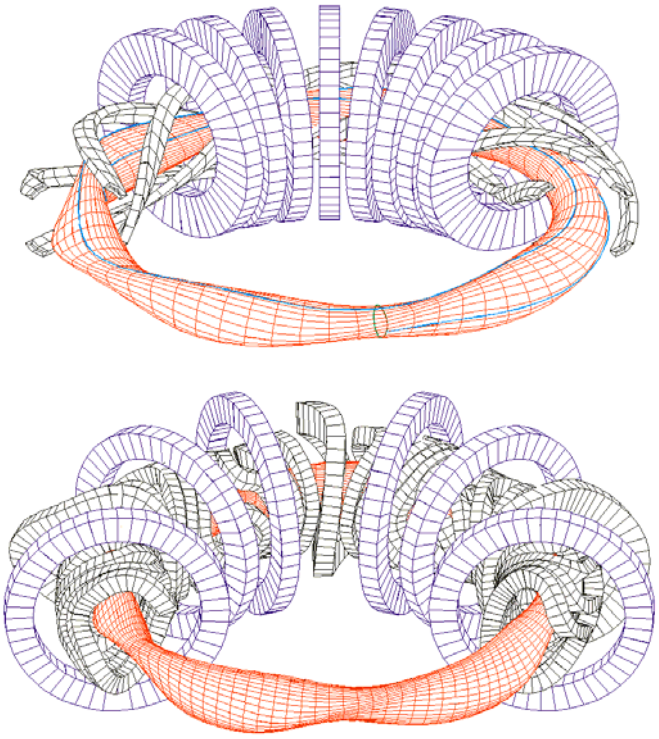
The Wendelstein 7-X concept





- Good nested magnetic surfaces and equilibrium properties at finite plasma pressure
- Good plasma stability
- Magnetic field largely independent of plasma pressure
- Good confinement of thermal plasma and fast ions
- Plasma exhaust concept for particles and energy (island divertor)

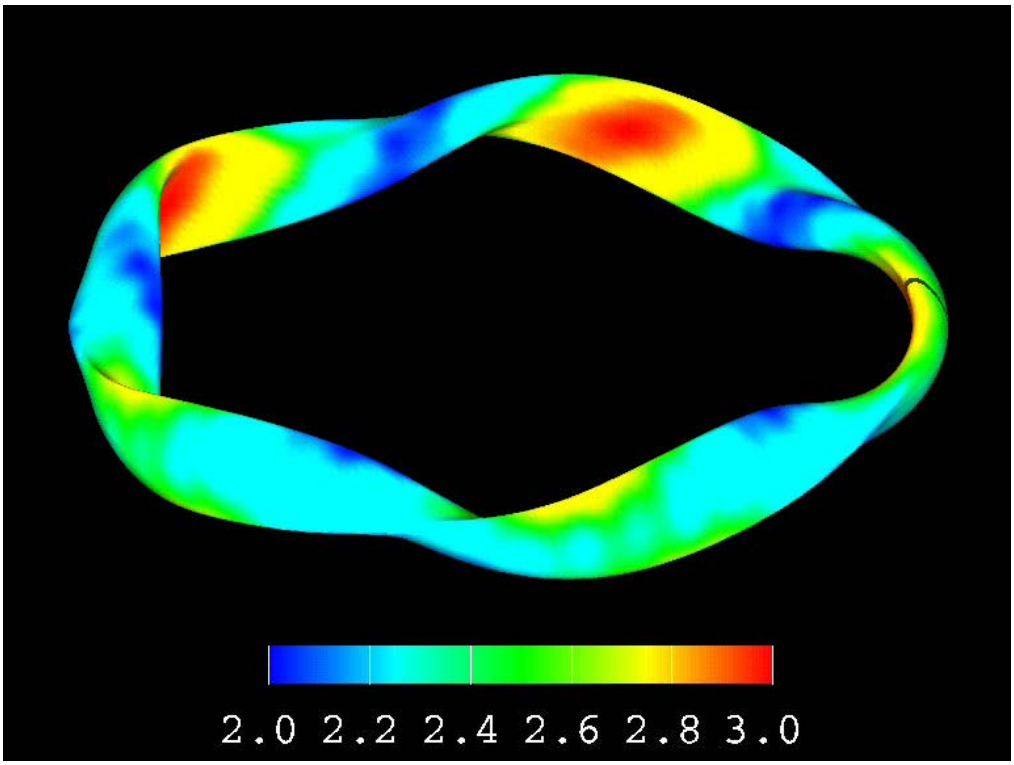
Classical versus optimized (advanced) stellarator



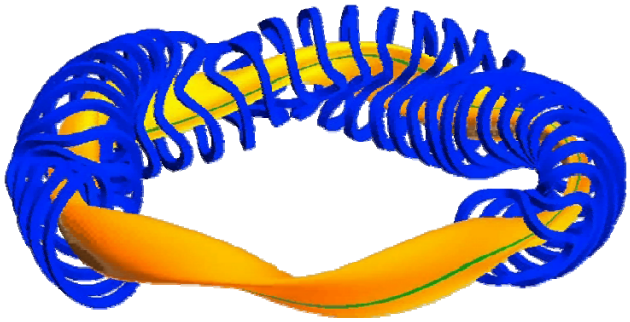
Modular coils allow tailoring (optimization) of magnetic field

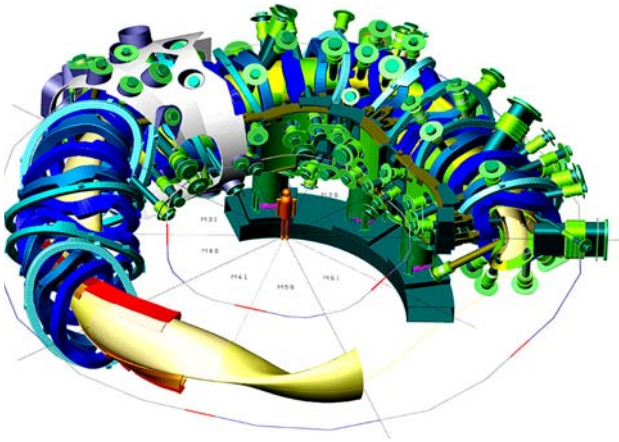
5 field periods:
Compromise between small curvature and minimizing number of coils

Good fast particle confinement (> 1 slowing down time) essential for a burning fusion plasma



Device parameters





Plasma volume ~ 30 m³
- major radius 5.5 m
- effective minor radius 0.55 m

Magnetic field 3 T
- magnetic energy 900 MJ

Superconducting coils
- 50 non-planar coils
- 20 planar coils

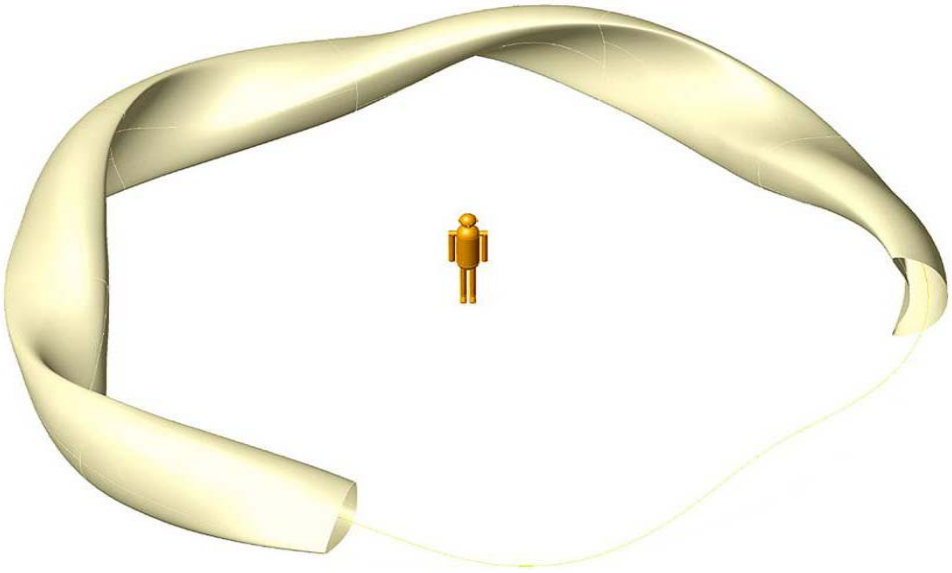
Pulse duration 30 minutes

Heating systems
- 10 MW ECRH (30 minutes)
- 20 MW NBI
- 12 MW ICRH

Actively cooled plasma facing components
- ≤ 10 MW/m²
- 10 MW cooling power

R. Wolf, SEI Tagung, Greifswald 22 September '08 17

Plasma



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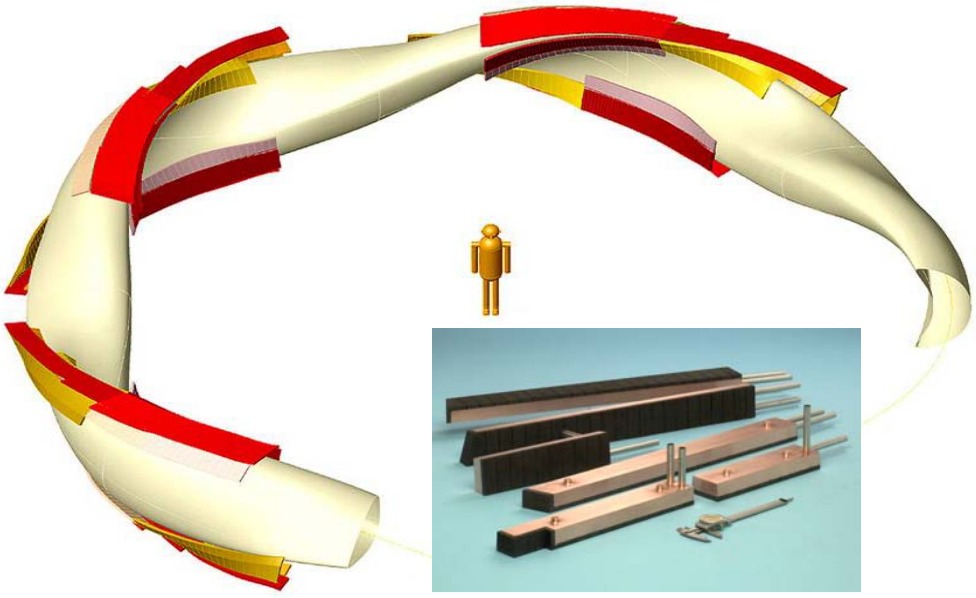
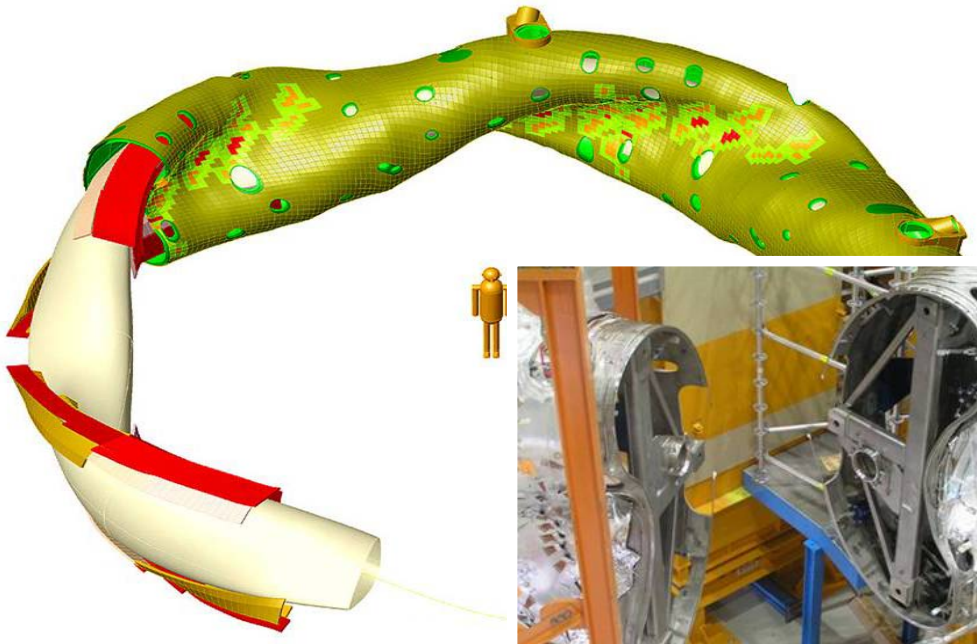
Plasma exhaust (divertor)

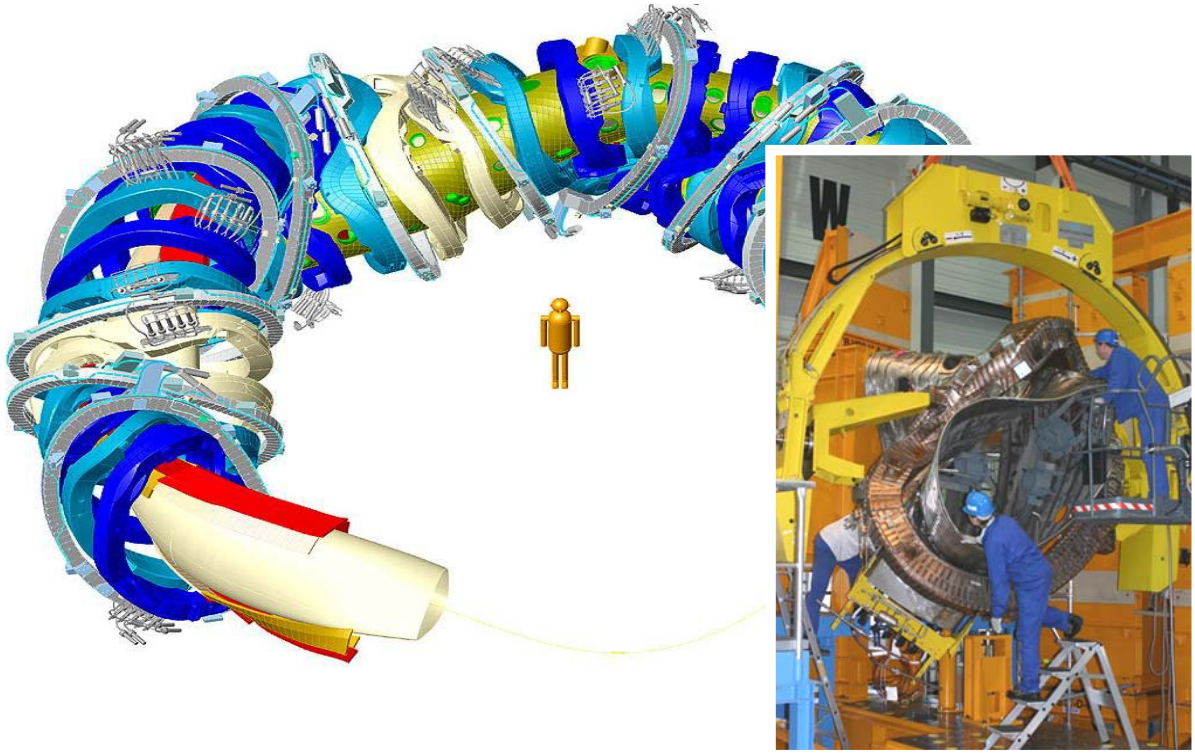


Actively cooled divertor elements
(up to 10 MW/m^2)

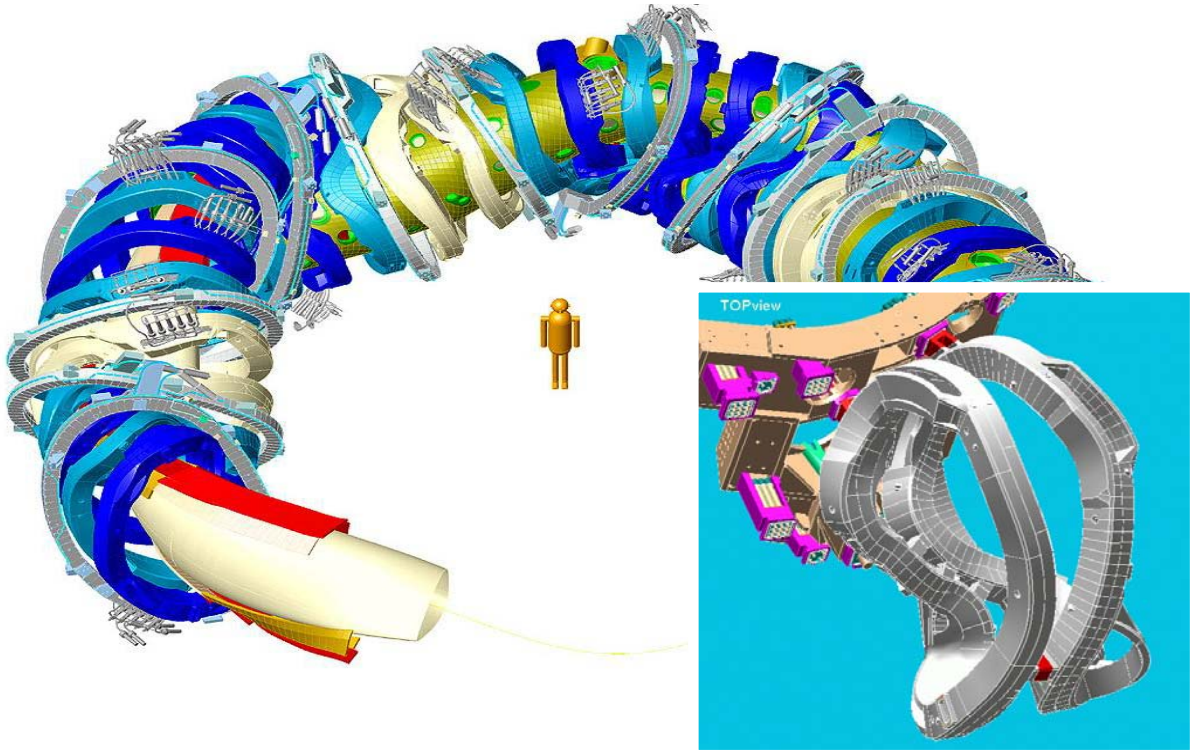
Plasma vessel



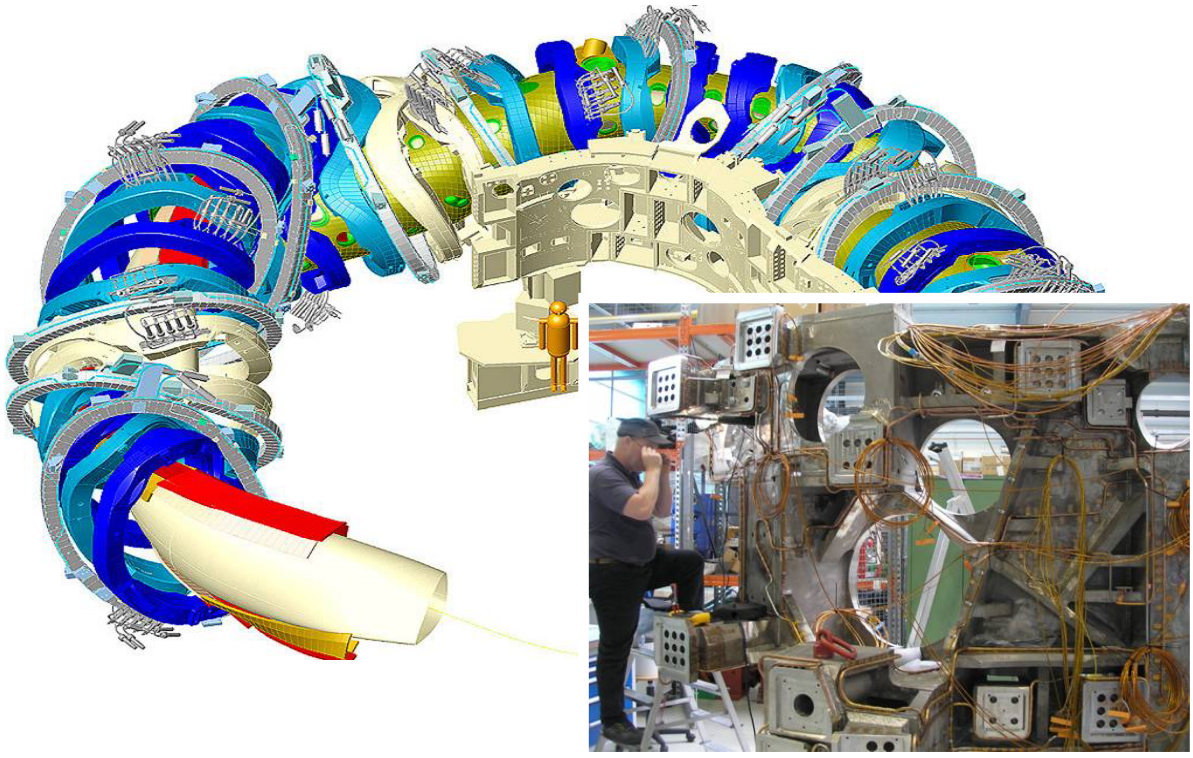
Coil system



Coil supports

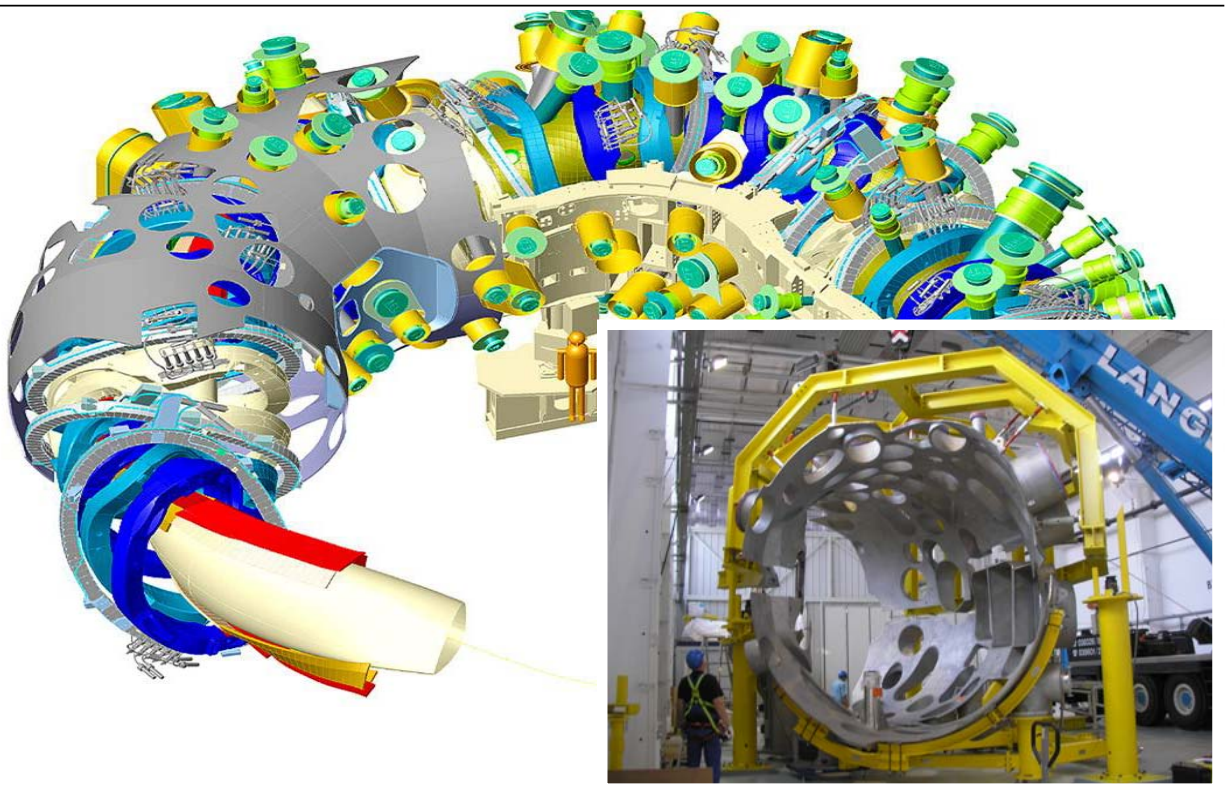


Central support structure



R. Wolf, SEI Tagung, Greifswald 22 September ‘08 23

Outer vessel of the cryostat and ports



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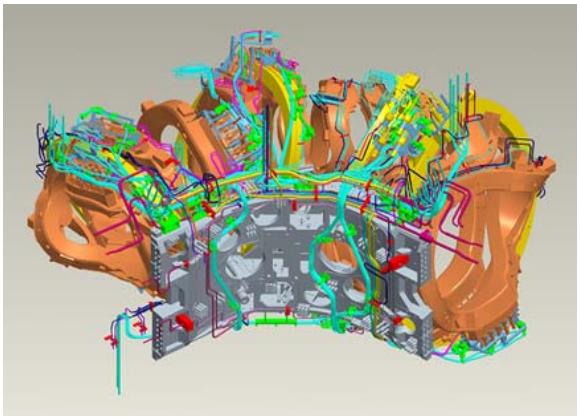
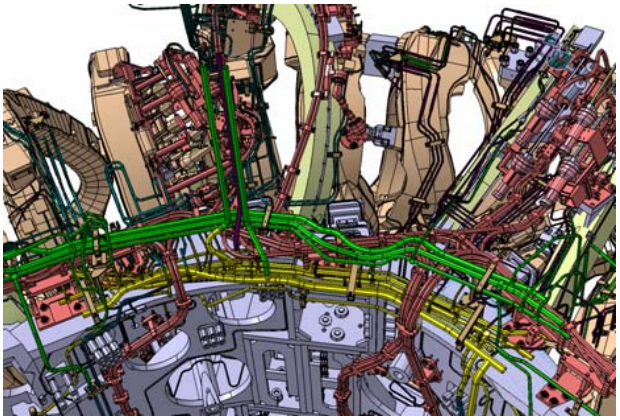
Busbars, helium pipes and instrumentation cables





JÜLICH
FORSCHUNGSZENTRUM

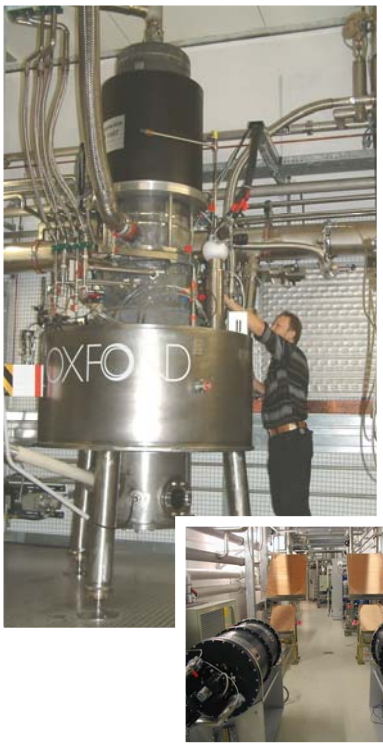
Steady state operation requires special …

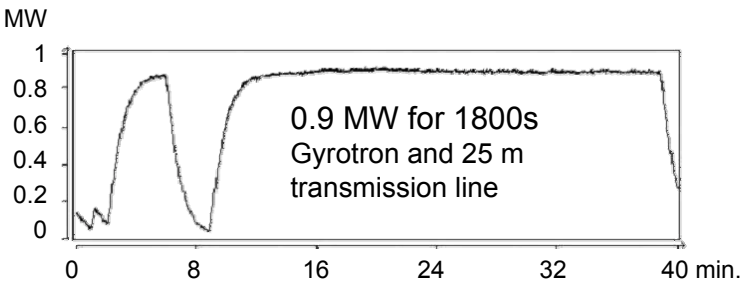
… control, data acquisition and real time data analysis

… plasma diagnostics

… heating systems

First demonstration of high power microwave heating





- 2nd harmonic electron cyclotron resonance heating
- 140 GHz at 2.5 T
- 10 × 1 MW for 30 minutes

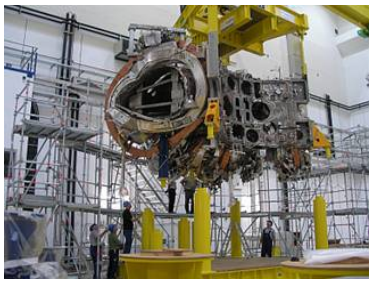
Forschungszentrum Karlsruhe
in der Helmholtz-Gemeinschaft

Universität Stuttgart

Assembly

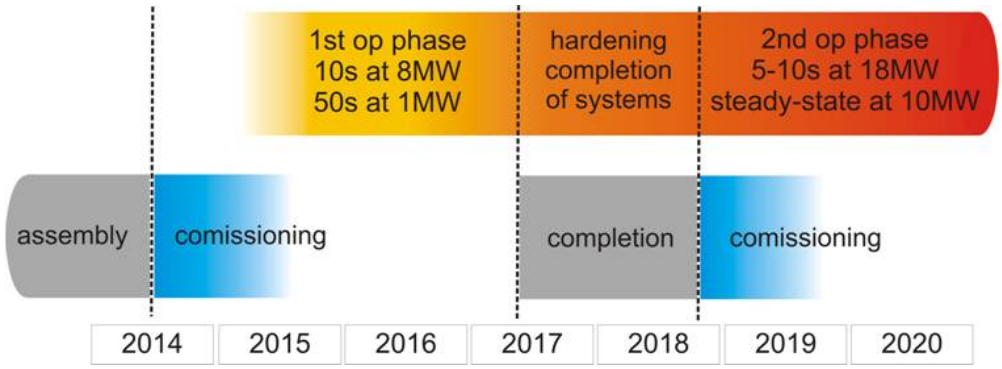
The first magnet module is mechanically complete,…

…transported in the experiment hall,…



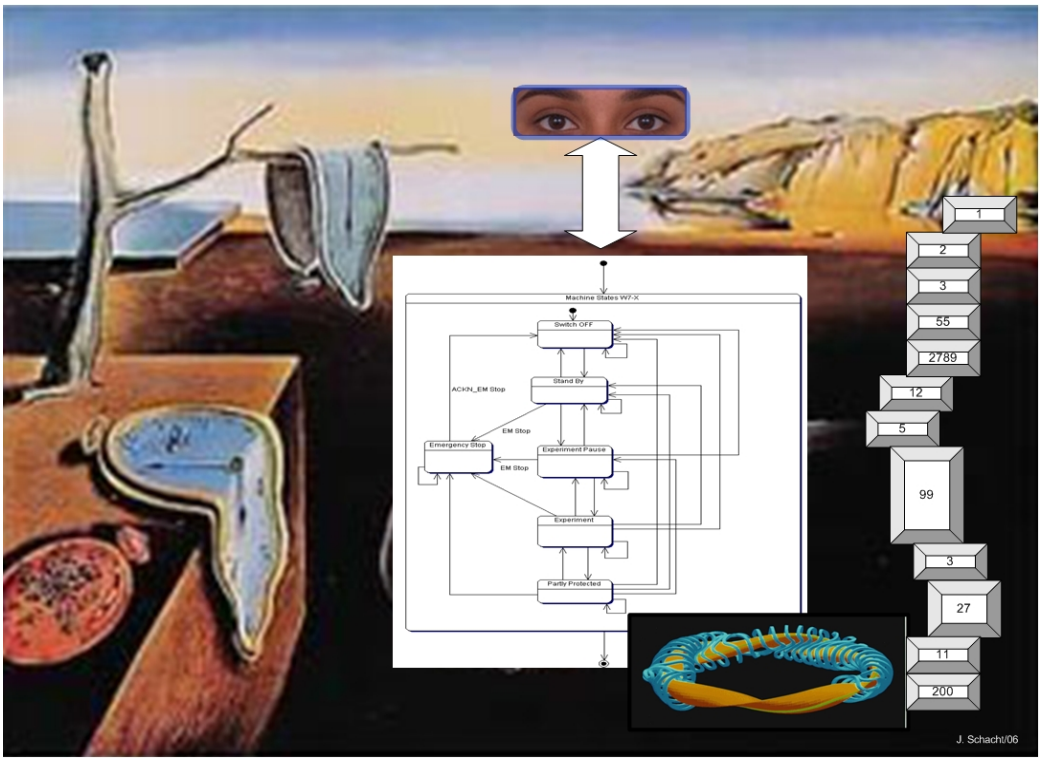
…and positioned on the next mounting stand (III) for the continuation of the installation of the bus-bars and helium pipes.

Schedule



- Assembly completed until May 2014 (simplifications)
- First plasma in May 2015
- 1st operation phase with un-cooled test-divertor unit → 8MW 10s discharges
- Device completion with actively cooled divertor, cooling circuits, ICRH and diagnostics
- 2nd operation phase with fully cooled in-vessel system → 10MW steady-state operation

Project „Prototype W7-X Control System”



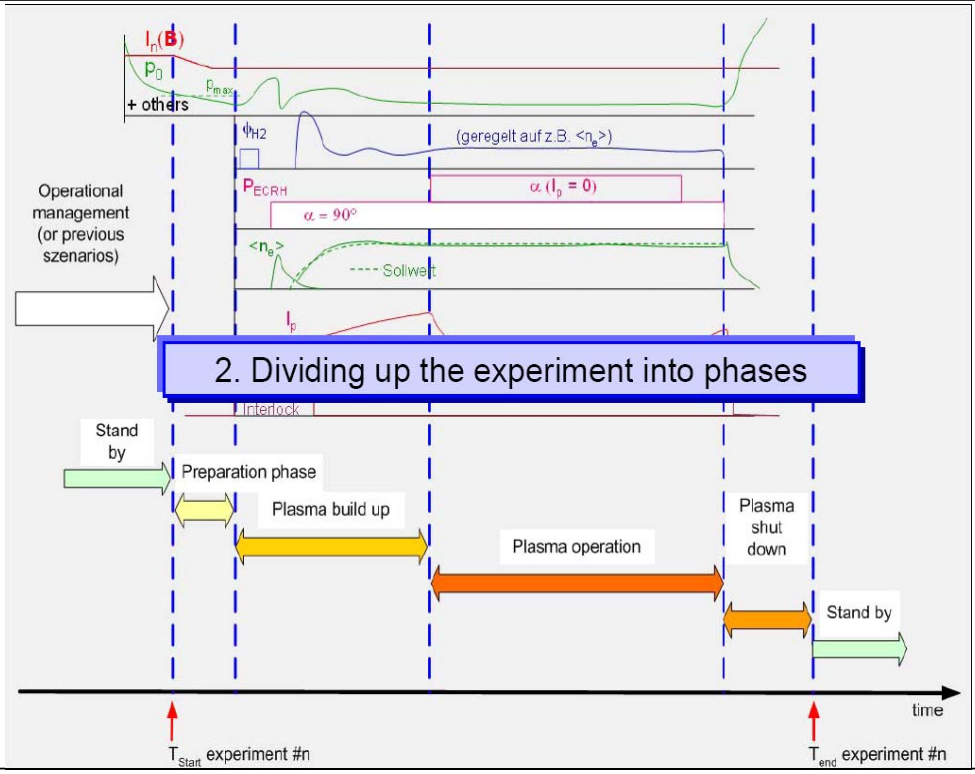
Project „Prototype W7-X Control System”

Outline

- ❑ **Short overview W7-X control concepts**
- ❑ **Project aims and background**
- ❑ **Test bed WEGA**
- ❑ **Project phase I and phase II**
- ❑ **Summary**

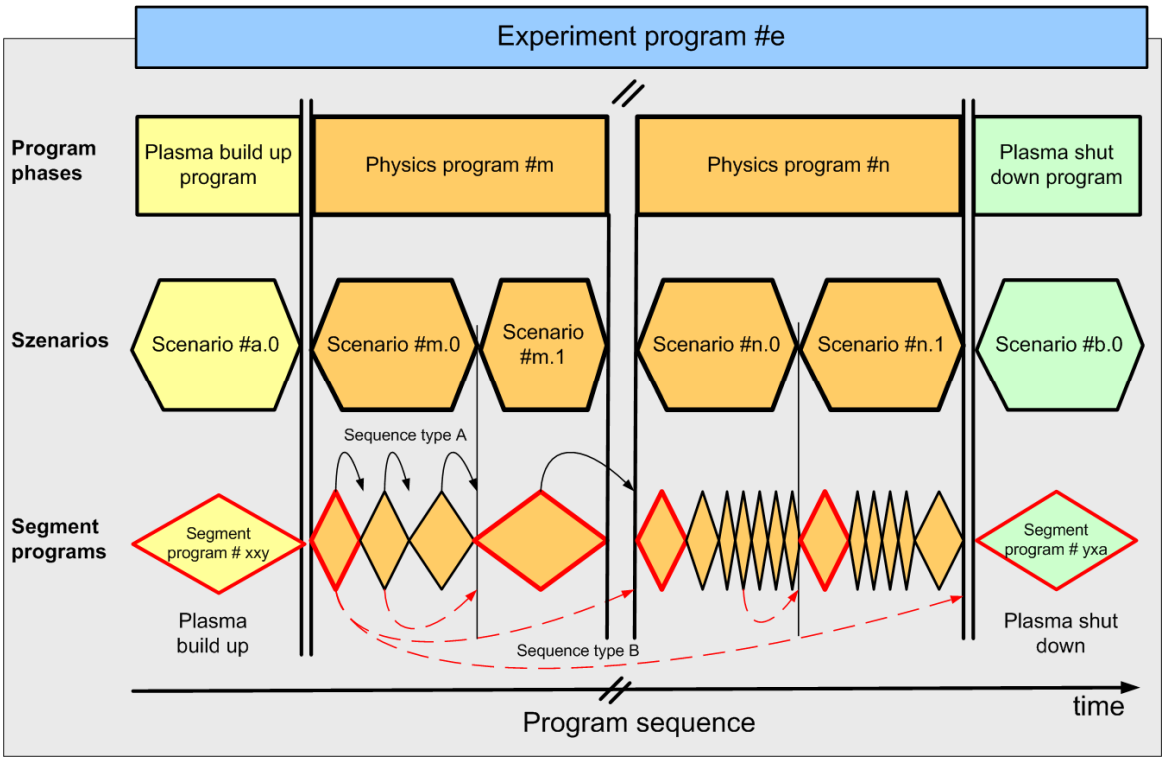
Project „Prototype W7-X Control System"

W7-X Control concepts: Segment control



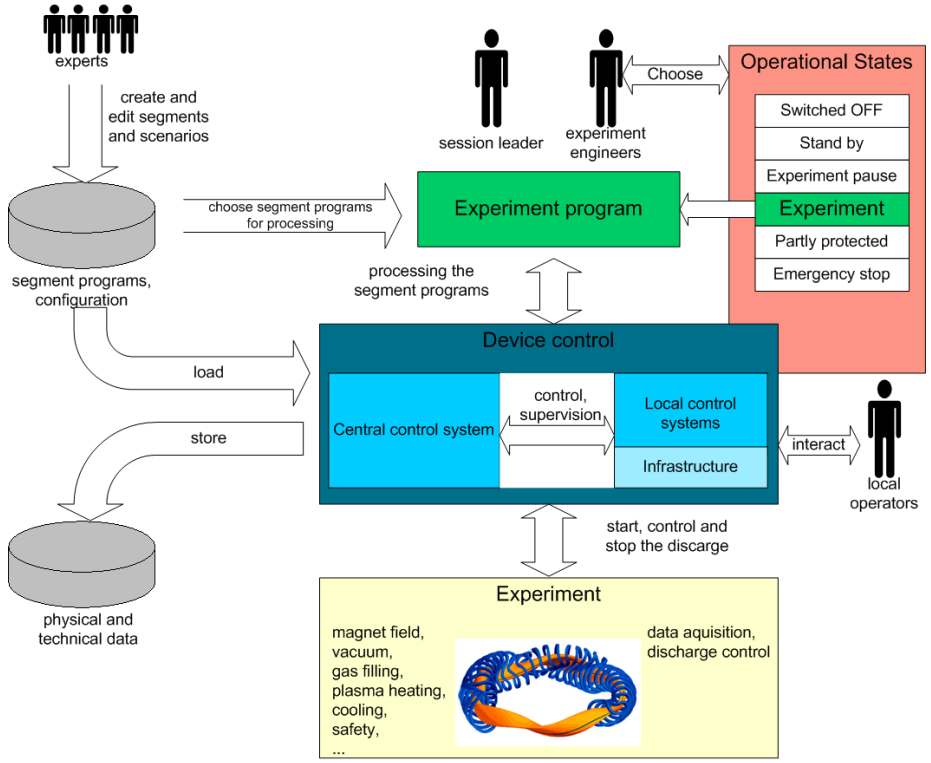
Project „Prototype W7-X Control System"

W7-X Control concepts: Experiment planning



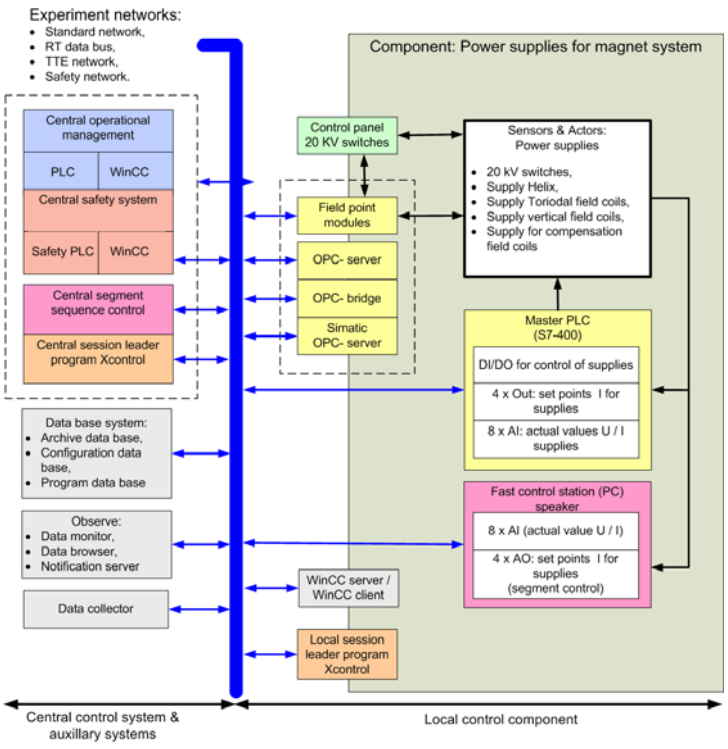
Project „Prototype W7-X Control System"

W7-X Control concepts: Segment program processing



Project „Prototype W7-X Control System"

W7-X Control concepts: Local control component (Magnet supplies)



Project „Prototype W7-X Control System”

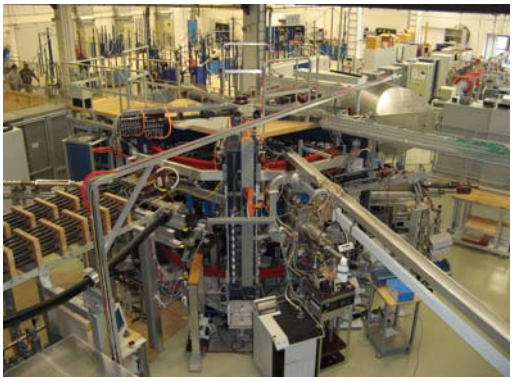
Project aims and background

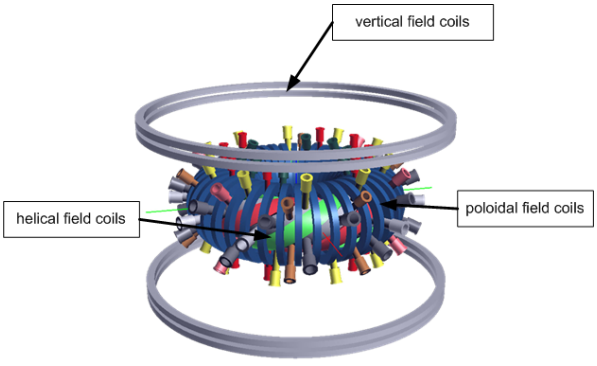
- Integrated test of control, data acquisition, diagnostics operation, heating and data processing in a W7-X like environment (steady-state segmented operation, scalability, real-time control, interplay with slow control of XDV, on-line data analysis tools) at an early stage,
- Demonstration of the W7-X operational safety concept,
- W7-X like routine operation: application of control concepts under plasma experiment conditions,
- Experience gain for department members of W7-X CoDaC,
- Optimization of the operational ergonomics (e.g. for session leader) & integration of component control,
- Early adoption of engineering and physics requirements with W7-X Control (e.g. test of feed-back density control),
- Distribution of expert knowledge to WEGA team and Technische Dienste,
- Early establishing of a test-bed for W7-X component commissioning (e.g. tests for remote operation without arbitrary access to torus hall)

A prototype test was a fundamental request of the reviewer of design review on march 2005!

Project „Prototype W7-X Control System”

Test bed WEGA





- Hybrid tokamak and stellarator experiment in Grenoble / France in the 70´s and 80´s for lower hybrid heating scenarios,
- Setup as classical stellarator at IPP Greifswald in 2000/2001,
- First plasma on 13 July 2001,
- May 2007: about 22000 discharges with a typical discharge time of 30 s,

Project „Prototype W7-X Control System”

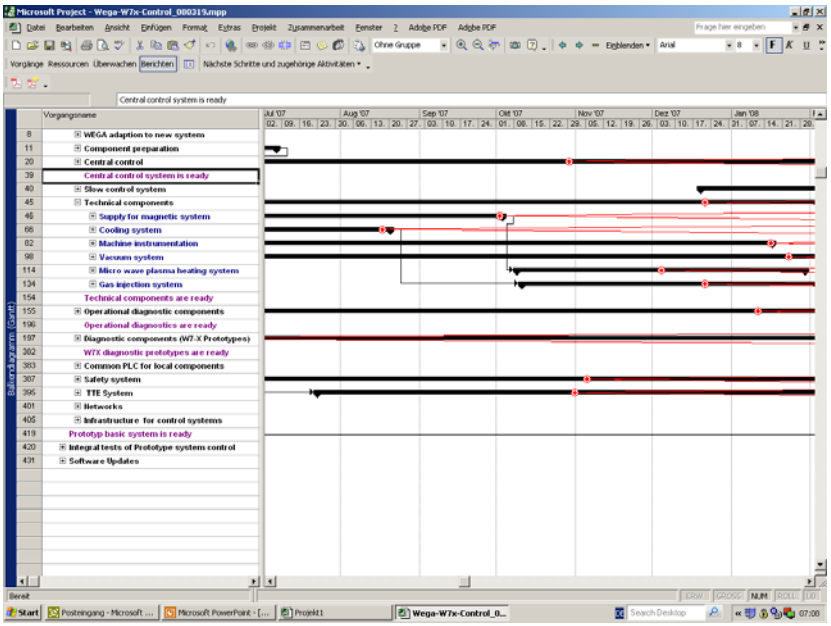
Project phases

- **Project phase 1: Implementation of W7-X control concepts**
  - Modification of WEGA control system
    - Signal switch unit (old control system ↔ new control system),
    - Planning, design and realization of new control components (WBS):
      - Central WEGA control system,
      - Safety system,
      - Technical components: Magnet supplies, cooling system, Micro waves heating system, vacuum system, gas inlet system,
      - Diagnostic components: Machine instrumentation, Density control, Spectrometry, Video diagnostics,
  - Time schedule: Oct. 06 → March. 08
- **Project phase 2: Operation, tests and physics operation**
  - Test and routine operation with new control system
  - Development and test of W7-X diagnostic prototypes
  - Time schedule: April08 → March 2010

Project „Prototype W7-X Control System”

WBS phase I + II

Standardization of WBS for design, construction, and tests of a component



Project „Prototype W7-X Control System”

Project structure

Base team:

Department	Department	Function
Machine Control	7	Head of project, Central and local operational management, Central and local segment control, FCS hard- and software, Safety System, Electro-technics,
WEGA	2	Deputy Head of project, Machine operation, Infrastructure, WEGA components
XDV	3	Local segment control, DAQ hard- and software,
TD electronic	2	Electronics and electro-technics
Diagnostic	2	Diagnostic experts
TD: Building service, mech. workshop, electro technique,	On demand	Fill orders

Project „Prototype W7-X Control System”

Project status

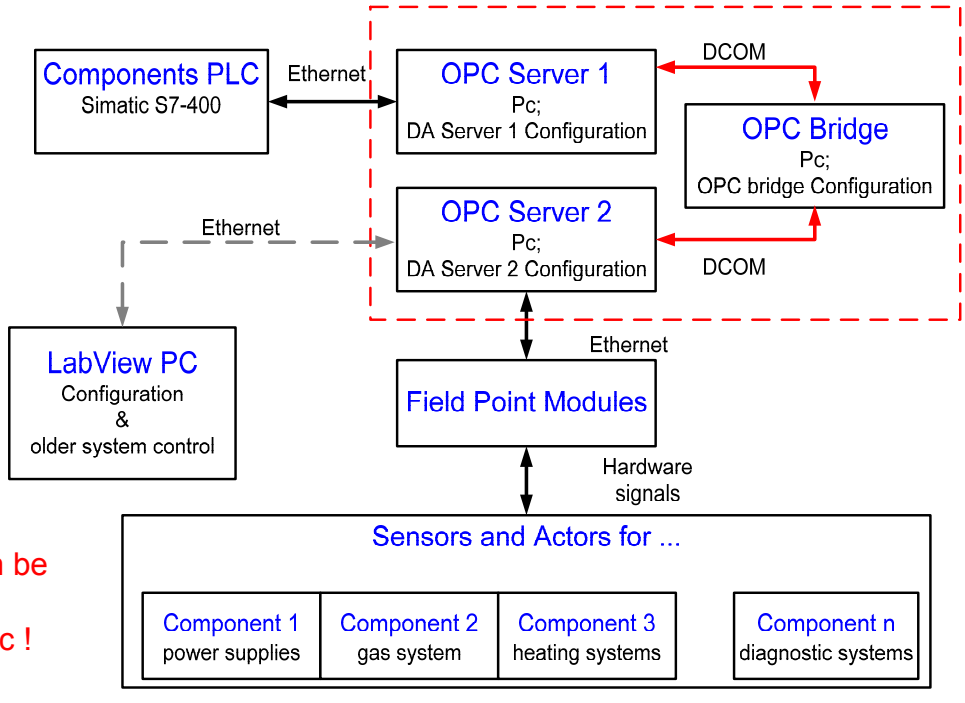
- **Realized technical components:**
  - Central control system, Safety system, Cooling system, Micro wave heating system, Gas injection system, Vacuum system
- **Realized diagnostic components:**
  - Machine instrumentation, Interferometer, Sopra echelle spectroscope, Stray radiation diagnostic,
- **W7-X diagnostic prototypes in realization or in planning:**
  - Magnetics, Neutral gas measurement, General purpose diagnostic, Integration of established WEGA diagnostics, Video diagnostic
- **Segment controlled experiment operation:**
  - WEGA standard discharge with Magnetron M1 and M2 (discharge time 35 s),
  - Long time discharge (discharge time **35 min** and **60 min**),
  - Multiple experiments in one discharge (discharge time 125 s),

Project meetings:

- one meeting every week,
- one “public” project meeting at beginning of a month
- actual 83 project meetings and a large number of technical meetings until now

Results: Integration of WEGA field level into the new control system

Hardware signal distribution using OPC technique



Cycle time can be in a range of about 0.5-2 sec !

Project „Prototype W7-X Control System”

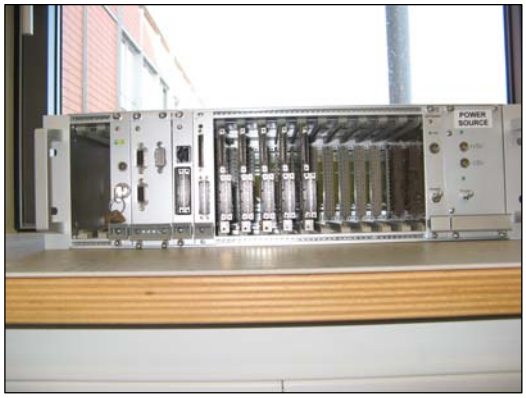
Results

- ET-Installations for control room and components infrastructure
  - design of el. cabinets done by project’s staff
  - Realization by TD Electronic (good quality, no financial effort for the project)
  - Installation tasks done by TD Haustechnik

Project „Prototype W7-X Control System”

Results

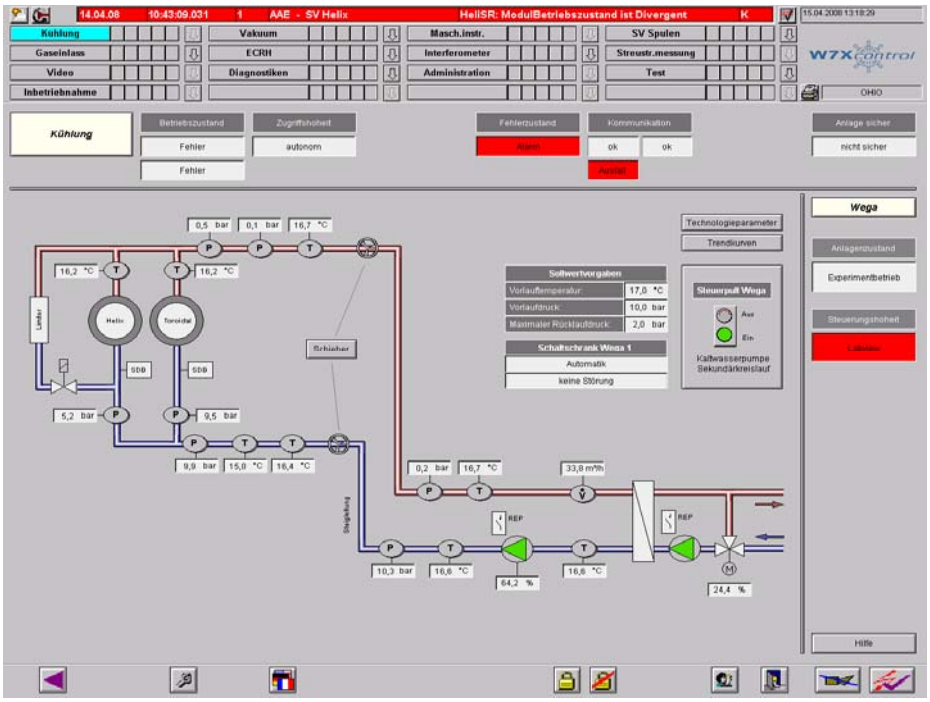
- Signal switch module system designed and built by TD Elektronik



Project „Prototype W7-X Control System”

Results

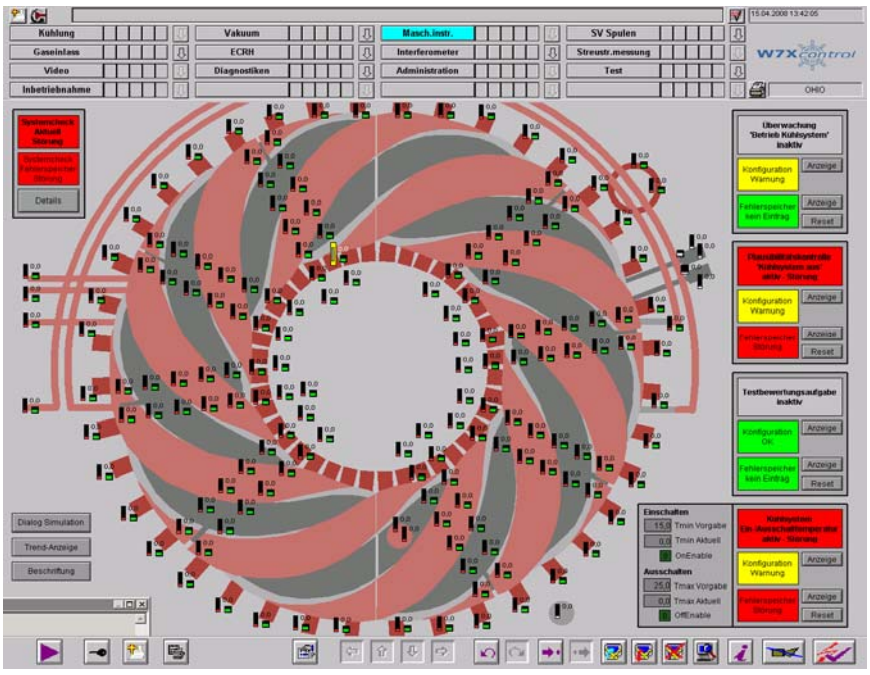
Visualization of IOPM Cooling System



Project „Prototype W7-X Control System”

Results

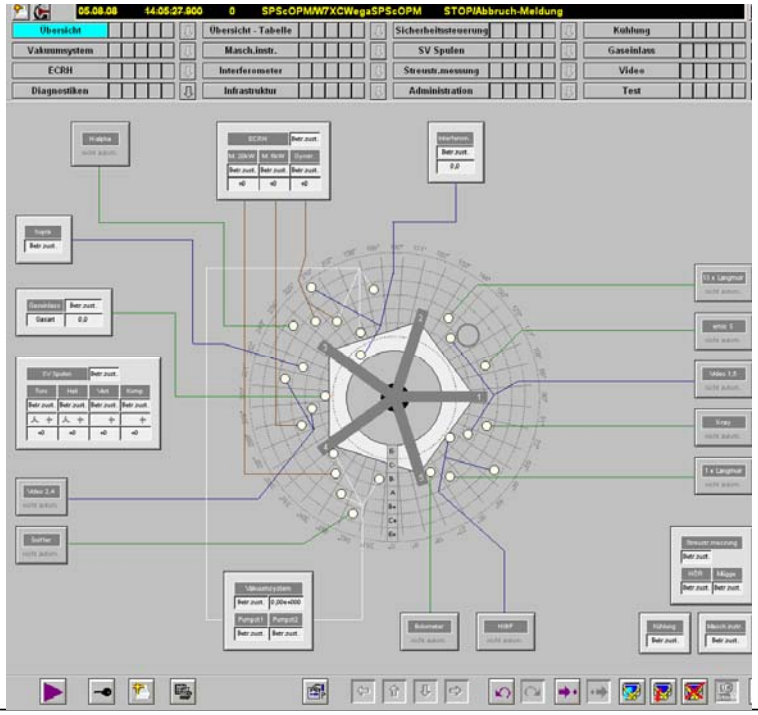
Visualization of IOPM Machine Instrumentation



Project „Prototype W7-X Control System”

Results

Visualization of cOPM WEGA



Project „Prototype W7-X Control System”

Results

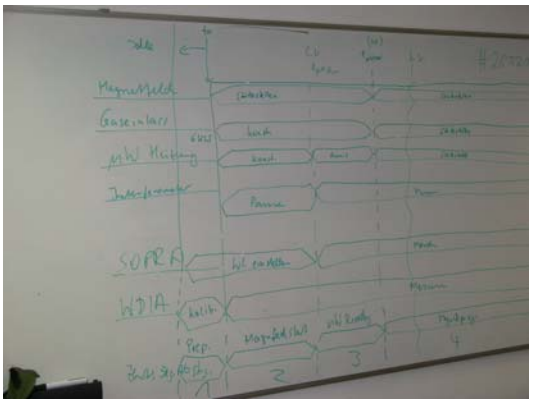
Safety System:

- Design and realization of Central Safety System,
- Implementation of Safety interfaces of components
- Commissioning and test of Safety System postponed to phase II

Project „Prototype W7-X Control System”

Results

First WEGA plasma experiment controlled by Segment Control
(beginning of April 2008)



Project „Prototype W7-X Control System”

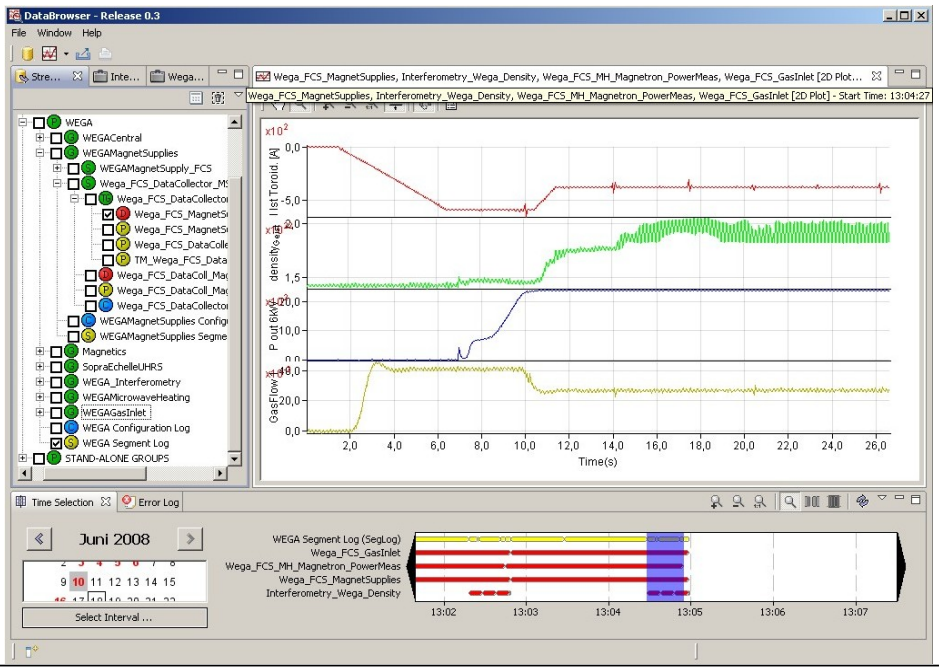
Results

The Milestone phase I reached on Friday, 11.4.08 at 14:45:
The plasma operation was successful!

Project „Prototype W7-X Control System"

Results

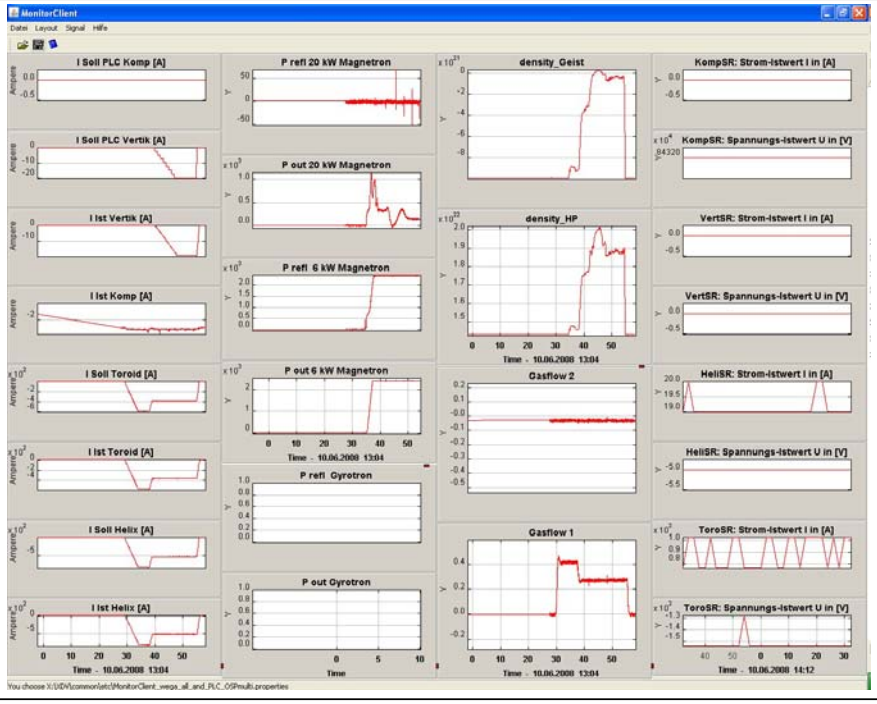
Archive data: Data traces of I_{Toro}, Density, $P_{Out,M1}$,Gas Flow visualized using the Data Browser Program



Project „Prototype W7-X Control System"

Results

Monitor data: Trend of different data streams



Project „Prototype W7-X Control System"
Review phase I

- **Summary phase I:**
  - All working packages realized,
  - Time and cost requirements for phase I fulfilled,
  - The design process of components done following a strict work flow
  - The existing concepts for control and data acquisition validated
  - The Integral Component Model for a control component successfully implemented
  - The WEGA running test operation
  - Education of personnel essential for phase II and W7-X project
- **Some tasks/tools/processes/… have to be optimized or are under construction!**

Project „Prototype W7-X Control System"
Phase II: Contain and plans

- **Components:**
  - Build up new components or extend existing components,
  - Acceptance tests for control components,
- **Safety System:**
  - Commissioning of safety interfaces, safety functions, and interlocks,
  - Acceptance test,
- **Plasma physics operation with segment control:**
  - Implementation of WEGA Standard Operation Scenarios:
    - Standard scenario 20KW Magnetron,
    - Standard scenario 6KW Magnetron,
    - Standard scenario 6KW + 20KW Magnetron,
    - High field operation with 28 GHz Gyrotron,
- ***Advanced control scenarios:***
  - *ECCD,*
  - *Density control,*

Participation of physicist :
• Optimization of tools,
•High Level Parameter concept,
•Clarification of daily workflow,
•Validation of control and data acquisition systems

Project „Prototype W7-X Control System”

Summary

- **Status:**
  - Phase I of the project accomplished by end of march 2008.
  - The WEGA project is now running in phase II.
- **Outlook:**
  - The focus will be set on test operation
- **To Do:**
  - take over the experiences of Prototype Project to W7-X!

Max-Planck-Institut für Plasmaphysik
EURATOM Association

Ein Serielles IO Konzept mit modularer DAQ Peripherie

K. Behler, H. Blank, A. Buhler, H. Eixenberger, M. Fitzek[1],
A. Lohs, K. Lüddecke[1], R. Merkel, G. Neu, G. Raupp,
G. Schramm, W. Treutterer, M. Zilker,
ASDEX Upgrade Team

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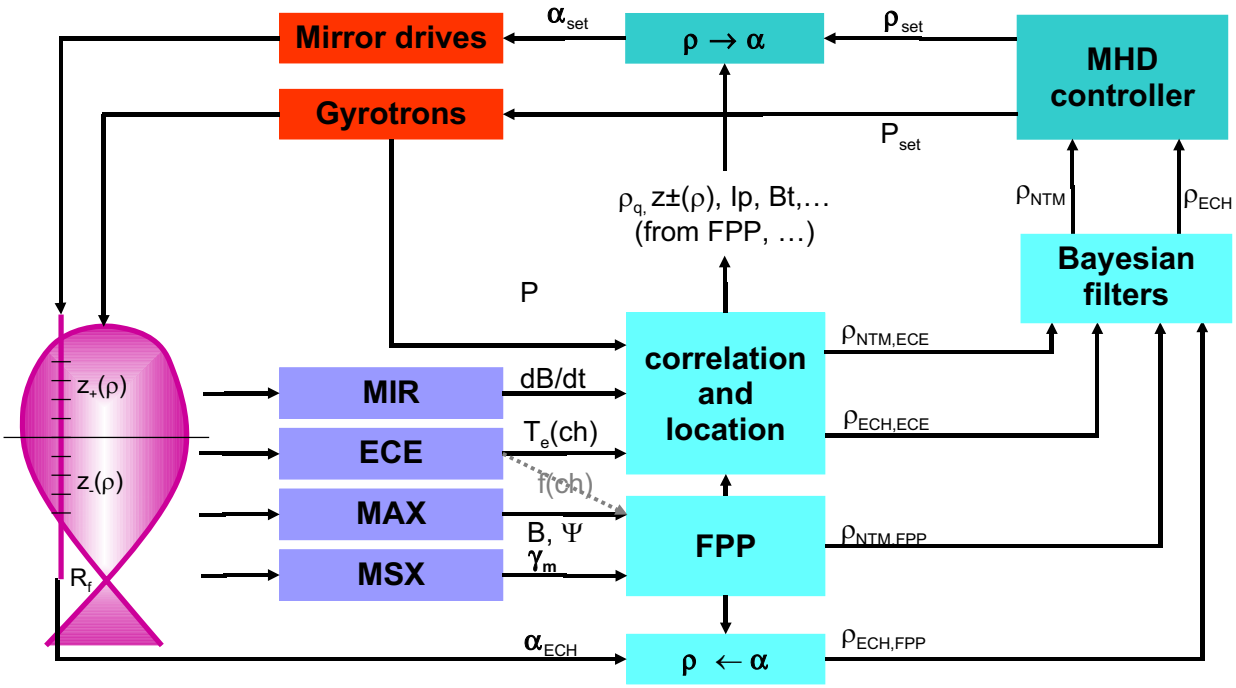
[1] UCS GmbH, Seeshaupter Straße 15, 82393 Iffeldorf, Germany

SEI Herbsttagung
22. September 2008, Greifswald

Gliederung

- Das Problem
- Anforderungen
- Ein Lösungskonzept
- Was schon da ist, was noch fehlt, und was nicht kommen wird.
- Zusammenfassung und Ausblick

Das Problemfeld: Feedback MHD Stabilization



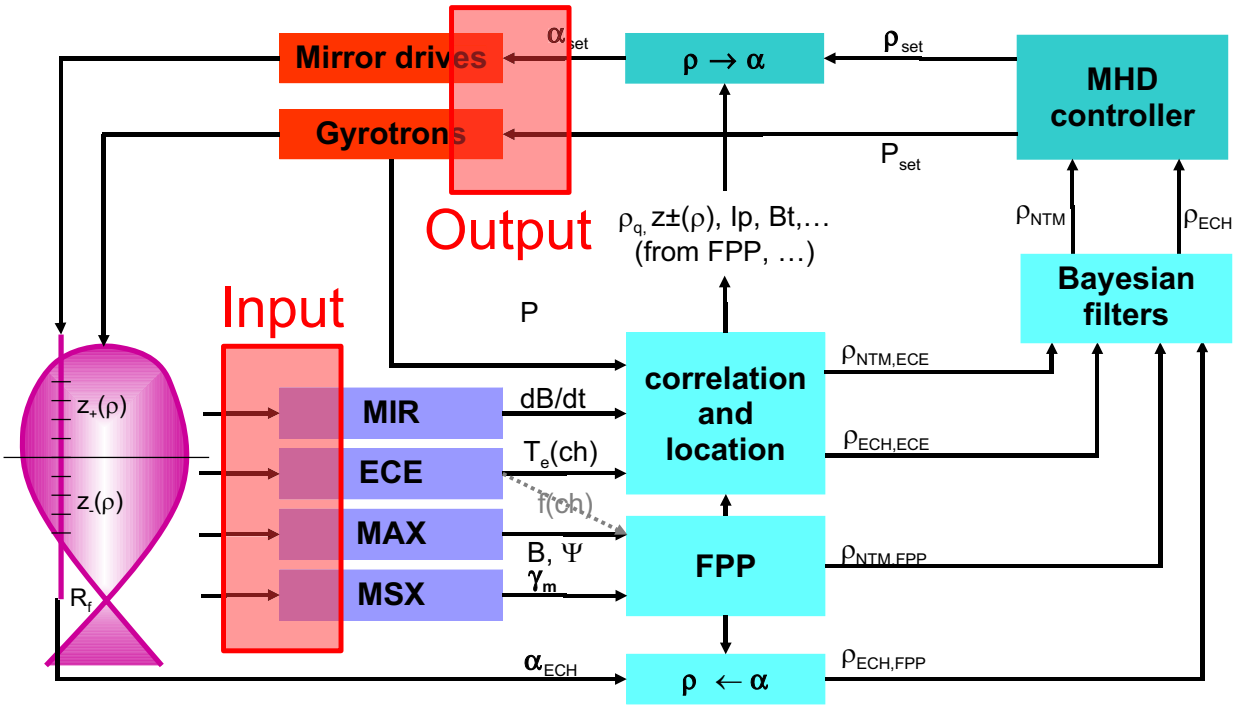
Die wesentlichen Herausforderungen

- verteiltes System, großes heterogenes Team
- breit gestreutes Spektrum an Sensorik (Standorte, Elektronik, Betrieb)
- sehr verschiedene Diagnostiken (Physik, Zeitverhalten, Auswertung)
- daten- und rechenintensive Mess- und Analyseprozesse
- komplexe und vernetzte Physik-Algorithmen
- kritische Kopplung mit der schnellen Plasmaregelung

Schwerpunkt des Vortrags
Elektronische Instrumentierung

Computerinterface mit modularer Analogperipherie

Positionierung des SIO Konzepts im Problemfeld



Warum das Rad neu erfinden? - Requirement Analyse

- “non-functional” Requirements
- Inputanforderungen
- Outputanforderungen
- Konfigurationsmöglichkeiten
- Online- und Selbsttestfähigkeit
- Zeitzuordnung und -erfassung
- Echtzeitfähigkeit
- Interface zum Rechner

“non-functional” Requirements

- Baukastensystem
  - Erweiterbarkeit
  - offen für neue Module, Sensoren, Algorithmen
- allgemeine Kriterien
  - billig
  - einfach
  - anpassbar
  - überschaubar
  - schnell erlernbar
  - nah am “Main Stream”

Inputanforderungen

- viele gleichartige Kanäle, kontinuierliches Sampling
  (Ende der Sensorbandbreiten oft bei 2 MHz)
  - Mirnov Sonden ADC 128x 2 MHz (Moden bis 400 kHz)
  - ECE ADC 64x 2 MHz
  - Soft-X-Ray ADC 256x 2 MHz (Turbulenzen)
  - Langmuir ADC 320x 2 MHz (Fluktuationen)
  - Überwachung ? 4096x 1-1000Hz
- besondere Isolation, Entkopplung und Erdung
- spezielle Sensoren, Sonderbeschaltungen
- nichtlineare, unmittelbare Messwertumformung
- regelbares Gain/Strom-/Spannungsversorgung, schaltbare Filter

Outputanforderungen

- Ausgabe zur Erzeugung von Analogsignalen (DAC) in Echtzeit
  - wenige Kanäle (typisch 16)
  - niedrige Taktraten (typisch 1-10 kHz)
- Veränderung von Konfigurationswerten in Echtzeit (parallel zur Datenerfassung, gleiche Samplingraten, determiniert)
  - Anpassung von Verstärkungsfaktoren
  - Änderung/Umschaltung von Samplingraten, Filterkoeffizienten, Kennlinien
  - Umschaltung von lokalen Algorithmen

Konfigurationsmöglichkeiten

- Konfigurationsmodus (off-line, seriell)
  - Adressierbarkeit jeder Karte und jeder einzelnen Komponente
  - schreib und lesbare Register und Speicher für Funktionsgruppen
    - Enable/Disable
    - Verstärkungsfaktoren
    - Filtereigenschaften
    - Kennlinien
  - “in place” ladbare Firmware (FPGA, DSP)
- Auslesen von Konfigurationsdaten
  - Betriebsmodi, Testergebnisse, Hardwarebeschreibung, Firmware read-out
- Messbetriebsmodus einschalten (echtzeitfähig, parallel, Neu-/Umkonfiguration nur in Taktpausen)

Online- und Selbsttestfähigkeit

- Prüfung der Funktionsfähigkeit
- Kalibrierung der Analogstufen
- Testmodus, evtl. mit DAC/ADC Gruppen
  (z.B. Signal über DAC erzeugen und über ADC einlesen)
  - Selbsttest der analogen und digitalen Baugruppen
  - Betriebssimulation durch simultane parallele Ausgabe und Aufnahme

zentrale Zeitzuordnung und Zeitnahme

- zeitliche Korrelation mit 20 ns erforderlich, stabil über lange Zeit
- verteilte Messsysteme (typ. 200 m Distanz), Laufzeitkorrektur

Vorhandene Lösung des Zeitproblems

- Zeitnahme durch gleichzeitiges Speichern von Zeit- und Messwert
  - lokale Counter laufen gekoppelt an einen zentralen Counter
  - gleichzeitiges Erfassen des lokalen Counters (TDC) und des Analogwerts
  - Datentyp “time-stamped sample packet”
  - zentraler Counter wird kodiert über LWL-Netz verteilt
  - zentrales Auslösung von Ereignissen
- Interrupt bei Erreichen eines voreingestellten Counts (Komparator)
- Speichern eines Counts auf Kommando (Zeitmessung per Software)
- Triggerpuls Erzeugung nach Kommando, Interrupt oder Programm
- interner Speicher für “gemessene” Zeitvektoren, auslesbar in Echtzeit

Resultierende Anforderung: eingebauter TDC

Echtzeitfähigkeit

- deterministisches Zeitverhalten
- “sofortige” Bereitstellung der Daten zur Verarbeitung
- “unmittelbarer” Weitertransport gemessener Daten
  - kurze Latenzzeiten
  - kleine Zwischenpuffer
  - DMA Fähigkeit (Effizienz und Unabhängigkeit von der CPU)
  - ausreichende Transferbandbreite
- Ausbreitung der Daten im Hauptspeicher eines Rechners
  - ausreichende Speicherbandbreite
  - schnelle Weiterverarbeitungsmöglichkeit
- Zugriffsmöglichkeit für Anwendungen (shared memory)

Interface zum Rechner

- **Kopplung eigenentwickelter Elektronik mit komplexer Rechnerhardware**
- Daten Handling
  - hohe Datentransferraten
  - Direct Memory Access möglich
  - Zwischenpufferung mit geringer Latenz
- Mechanische Eigenschaften, Format
  - modular, gut zugänglich, zuverlässig steckbar, flexible Anzahl von Steckplätzen
  - leicht anpassbar an neue Rechner-/Bustypen (mitschwimmen im Mainstream)
- Programmierung
  - Treiber für multiple Betriebssysteme
  - Einheitliche Anwendungsschnittstelle für portable Anwendungssoftware

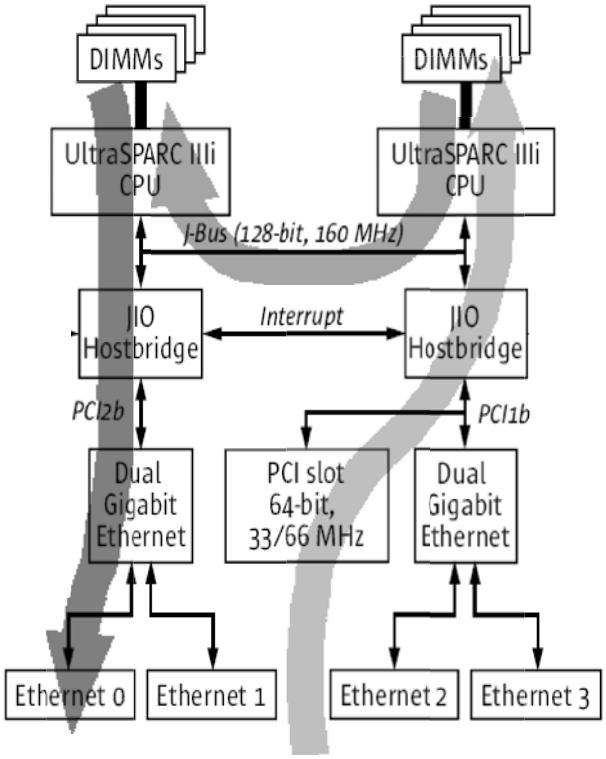
How to get something into a computer - FAST

→ Direct Delivery of Data into computer memory

- Transfer driven by external DMA devices
- Minimized latency (CPU-cache sync. required)
- Setting CPU power free
  1st CPU is >50% empty
  2nd CPU is 100% empty
- Using internal communication pathes, memory bandwidth and CPU power most efficiently

Free capacity for

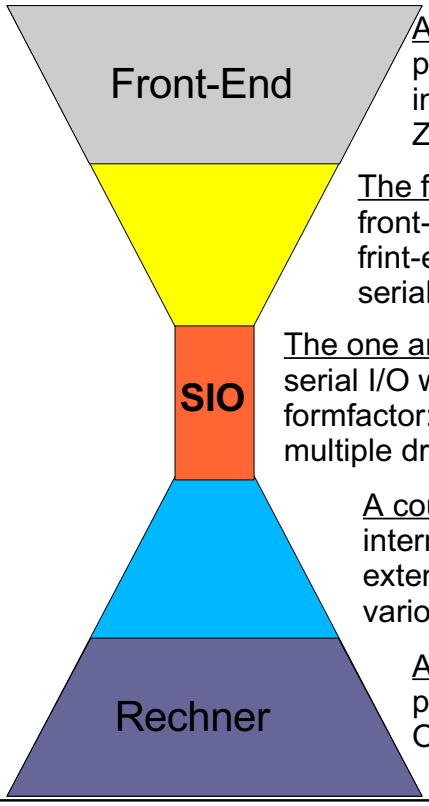
RT Analysis



Vorgeschichte

- 80er Jahre Transputer-Links (Hertweck et al., Raupp/Richter, ...)
  Transputer-Rechner mit seriellen Links zur Peripherie
  Selbstbau Eingangsstufen mit seriellen Transputer-Links
- Ende der 90er HOTlink 1
  Standardrechner mit PCI-bus
  PCI-karten mit 8x HOTlink 1 (alternativ PCI-Karten mit Transputer-Links)
  Selbstbau Eingangsstufen mit HOTlink 1 (Umbau der alten Eingangsstufen)
- Entwicklung der Pipeline als Träger und Multiplexer für Analogperipherie

Das heutige Konzept hat fünf Schichten



A broad variety of front-end devices:
pipelined backplane: ADCs, Scaler, Framegrabber
integrator backplane: AUG MAG integrators
ZTE backplane: bridge-amplifier ADCs

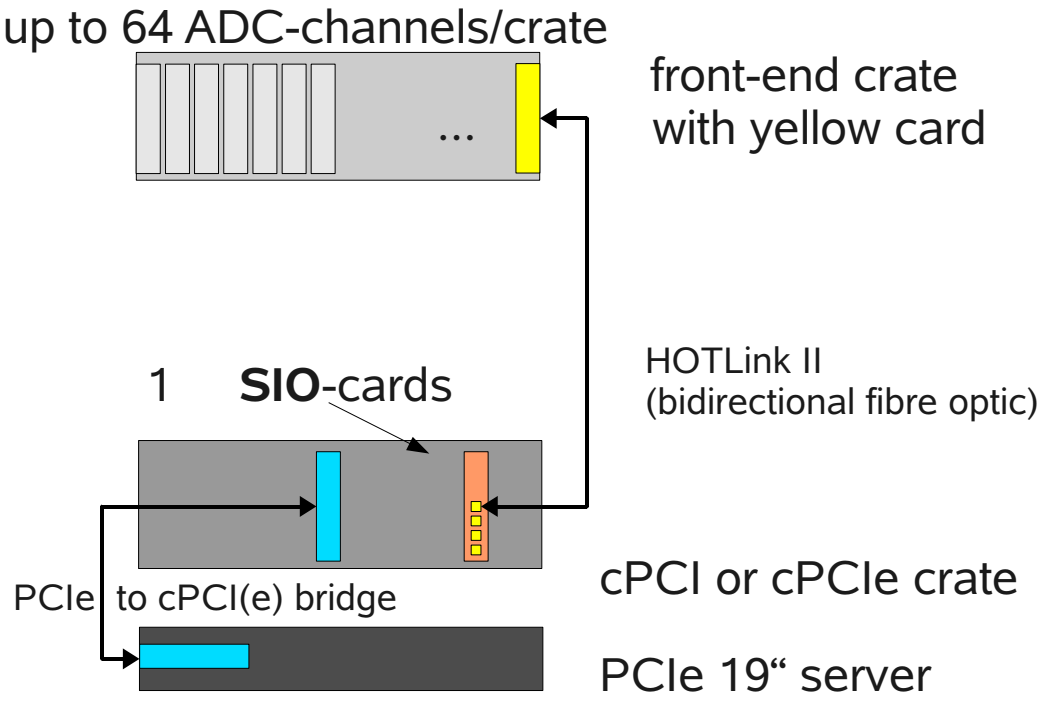
The front-end adapter card:
front-end interface: pipeline or other
frint-end protocol: pipeline or other (FPGA programmable)
serial up/down link: HOTLink II (optical fibre)

The one and only computer interface:
serial I/O with 4x HOTLink II, FPGA & embedded TDC
formfactor: compact PCI or compact PCIexpress
multiple drivers: LINUX, SOLARIS, Windows, VxWorks

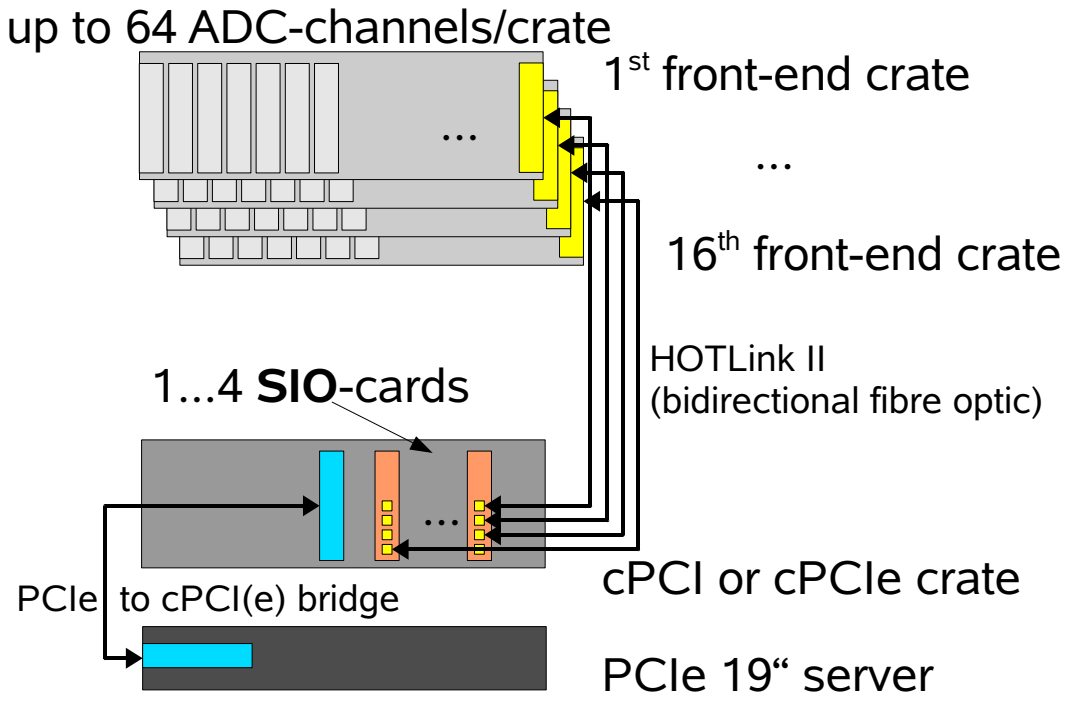
A couple of computer interface busses:
internal: PCI-bus, PCIe-bus, (S-bus, VME-bus ...)
extensions: cPCI, cPCIe, (PXI, VME ...)
various bridges: PCI-cPCI, PCIe-cPCI, PCIe-cPCIe

A broad selection of computer platforms:
processors: AMD, Intel, SPARC
OS choices: LINUX, SOLARIS, Windows, VxWorks

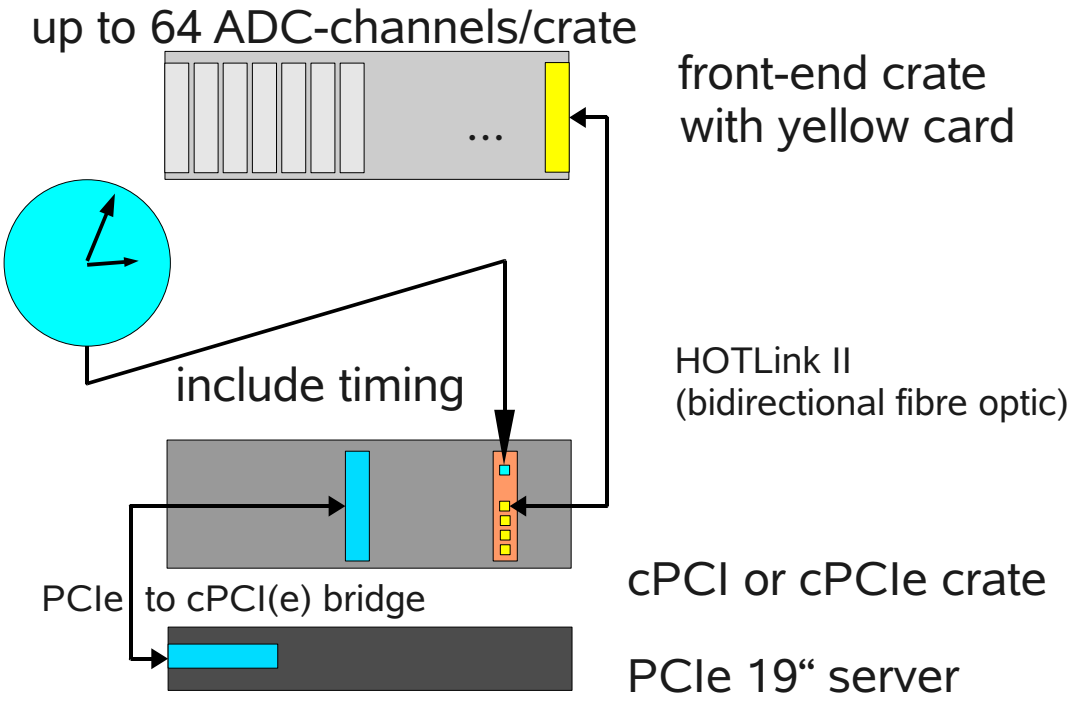
HOTLink II SIO Interface und Pipeline Front-End



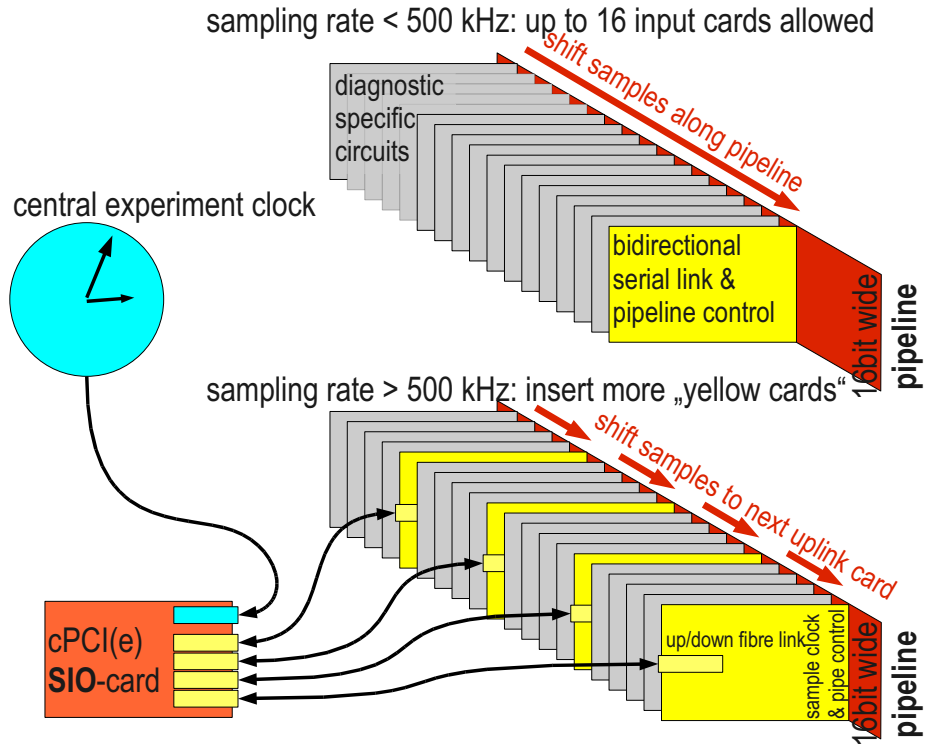
Erweiterbarkeit bis 1024 Kanäle (und mehr)



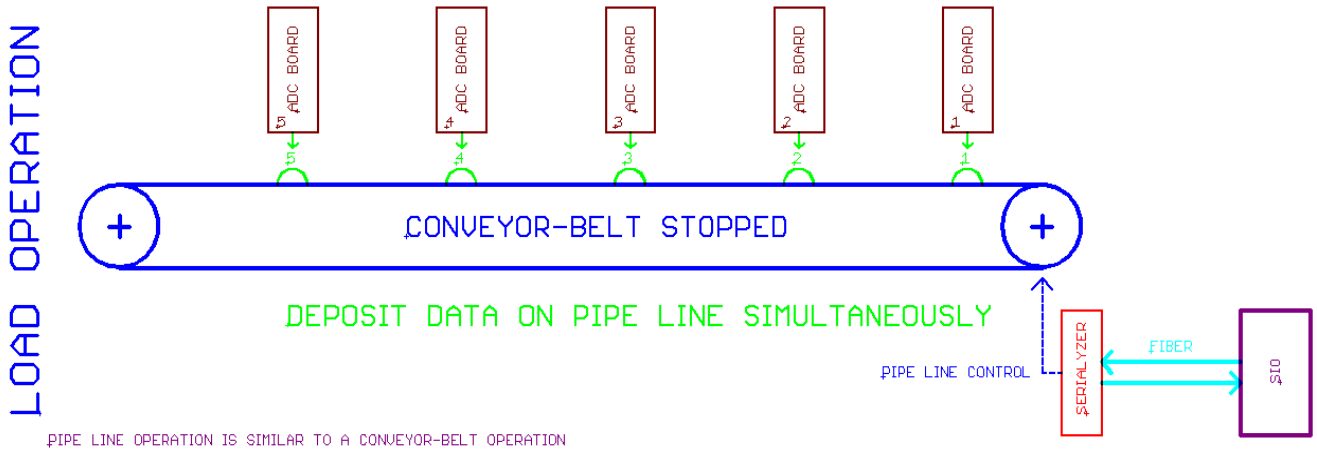
SIO Interface mit zentraler Zeitsynchronisierung



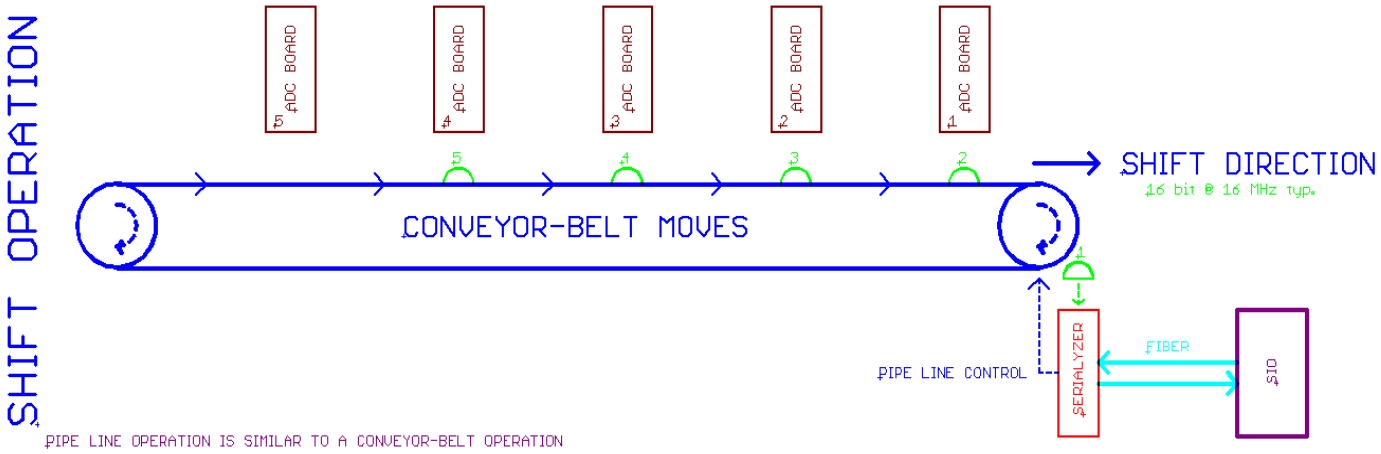
SIO Karte mit vorgeschalteter Pipeline-Backplane



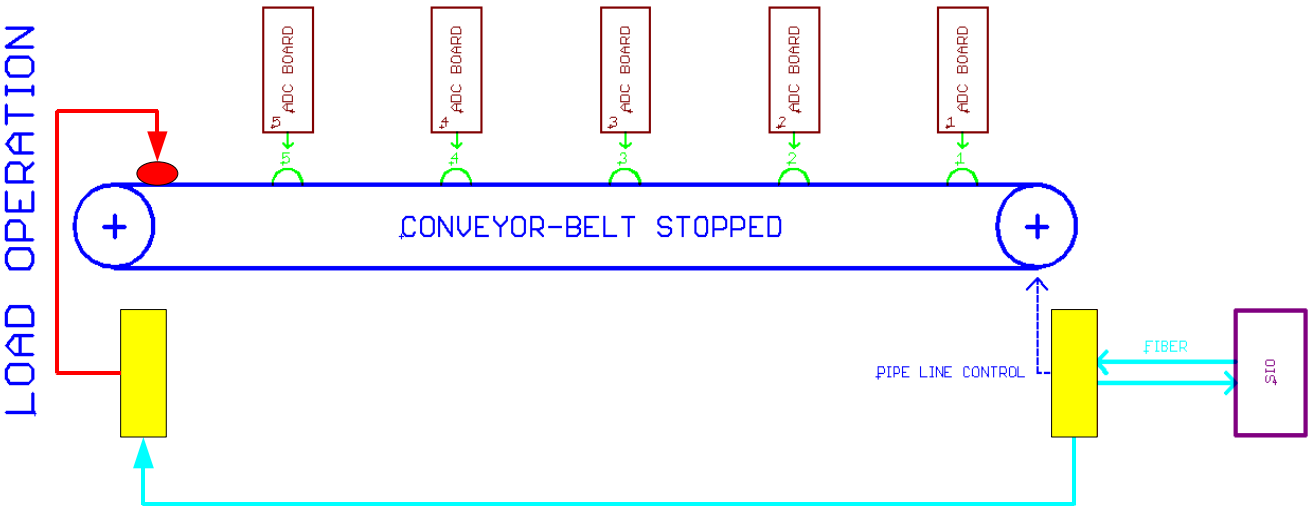
Arbeitsweise der Pipeline
1. Schritt: Daten ablegen



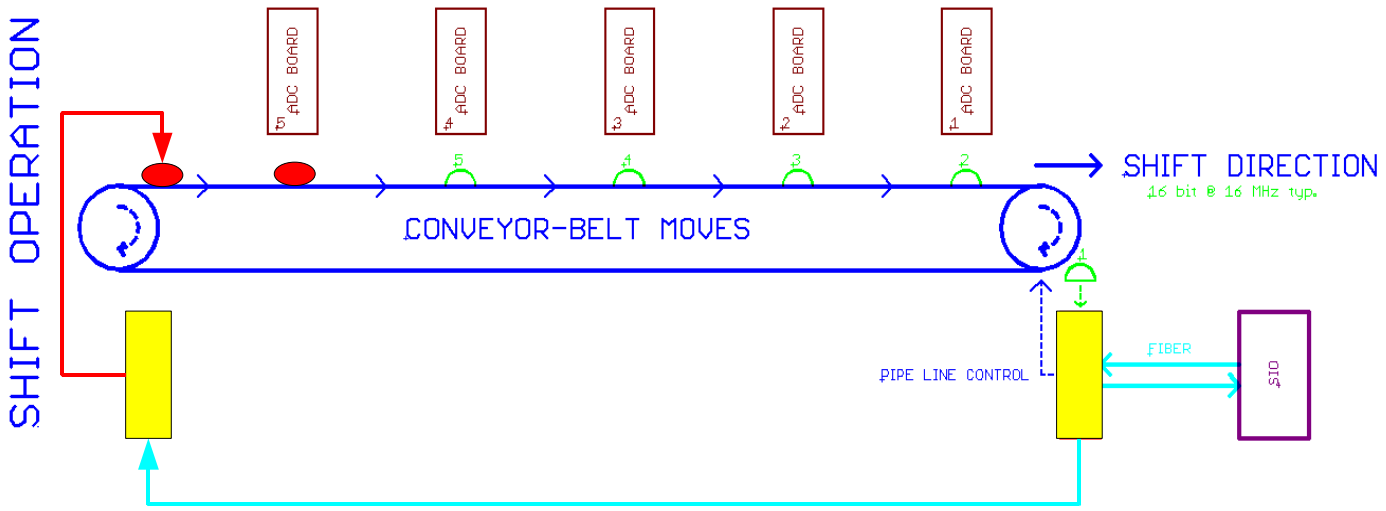
Arbeitsweise der Pipeline
2. - n. Schritt: Daten transportieren



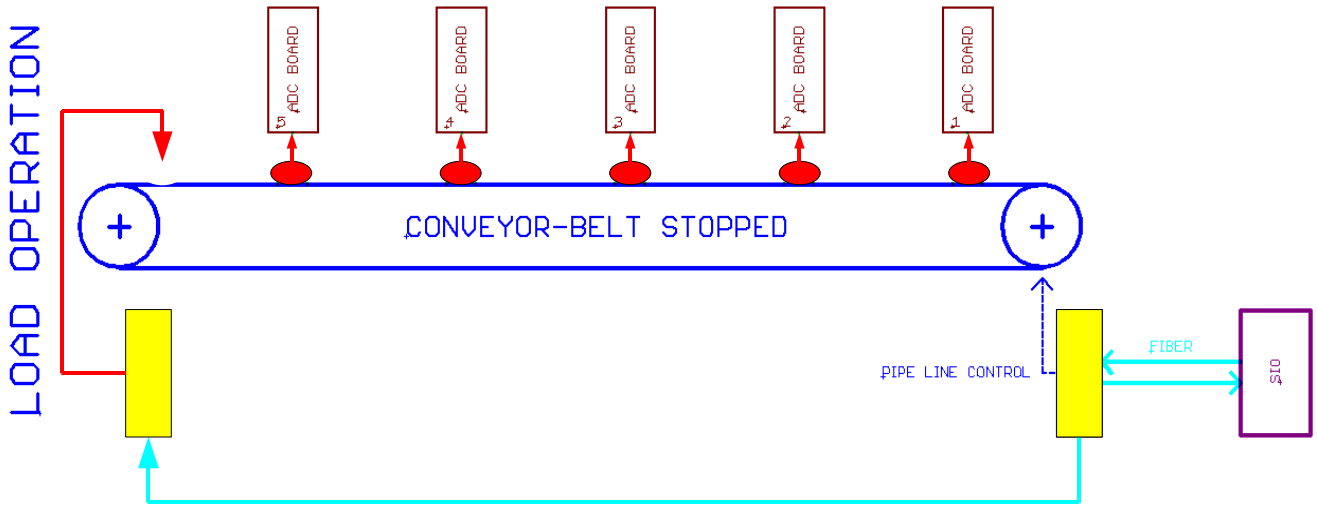
Arbeitsweise der Pipeline (gleichzeitig Input & Output)
1. Schritt: Daten gleichzeitig ablegen



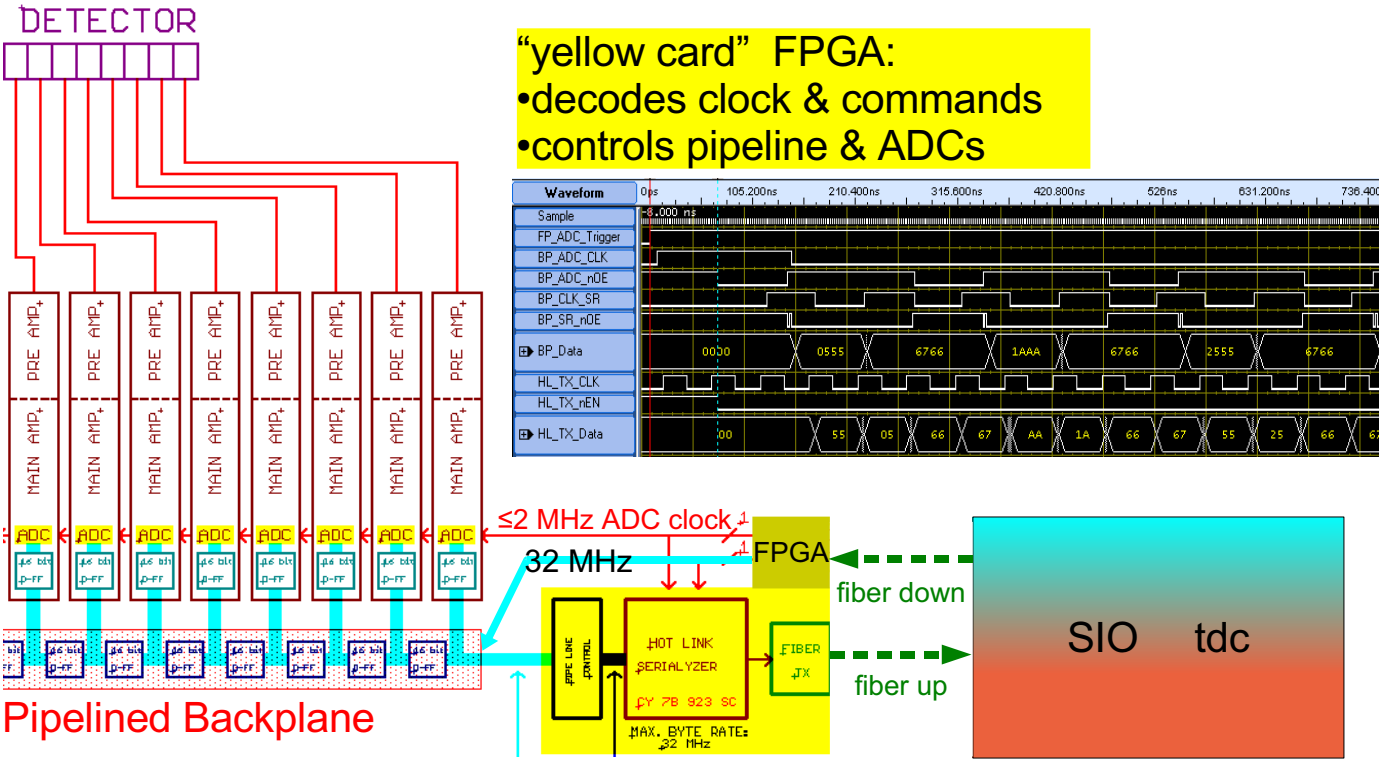
Arbeitsweise der Pipeline (gleichzeitig Input & Output)
2. - n. Schritt: Daten transportieren & nachschieben



Arbeitsweise der Pipeline (gleichzeitig Input & Output)
letzter Schritt: Output-Daten laden

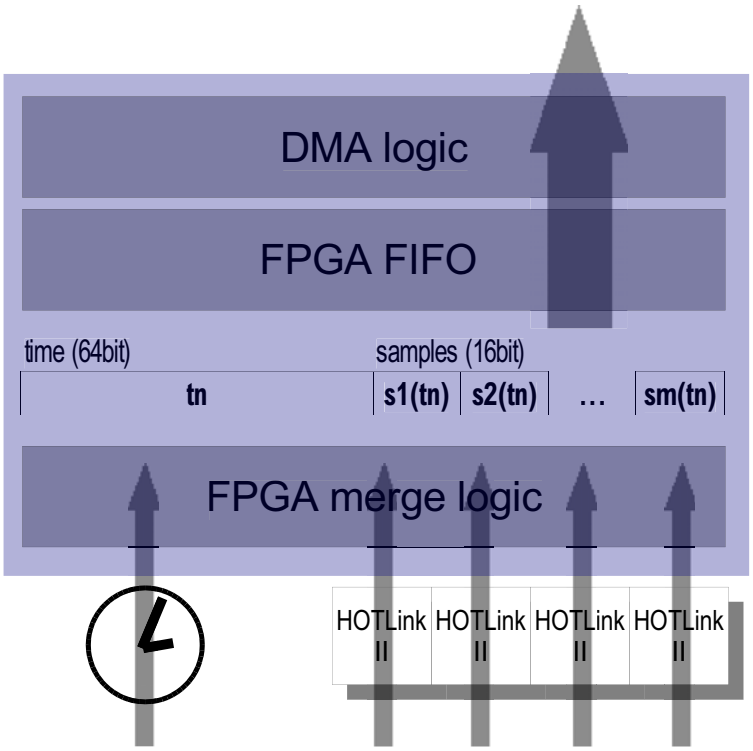


Yellow Card derives local clock from SIO tdc clock



SIO FPGA merges samples & time

Creating a single stream of time stamped data frames.



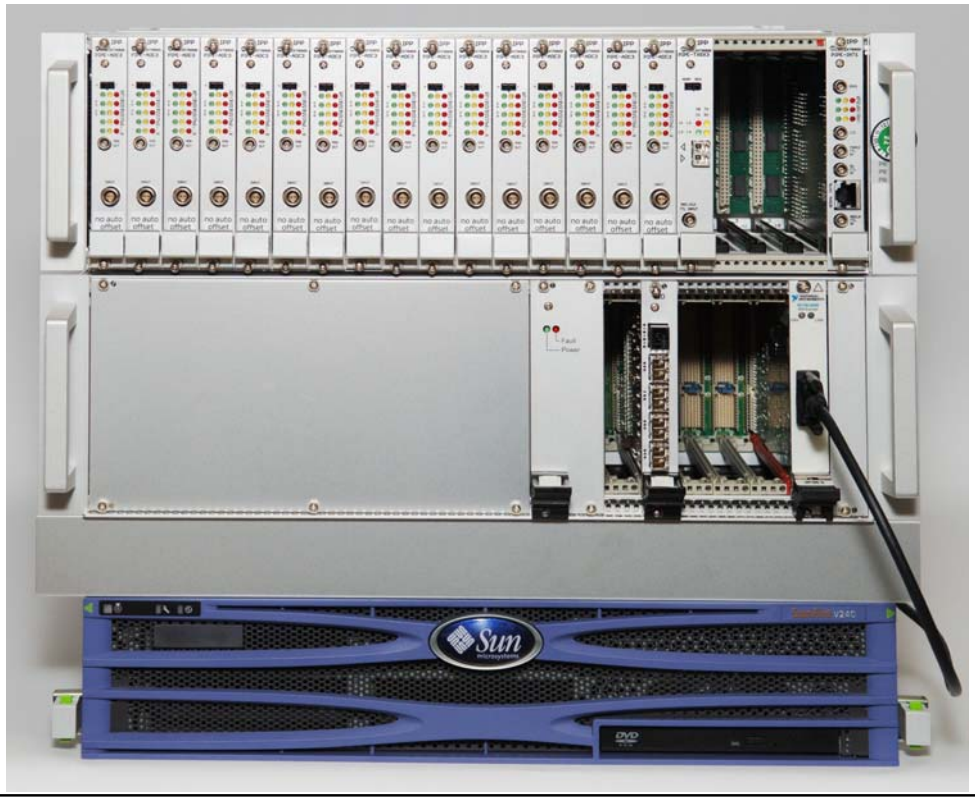
SIO data frame format combining:

1 stream of time stamps

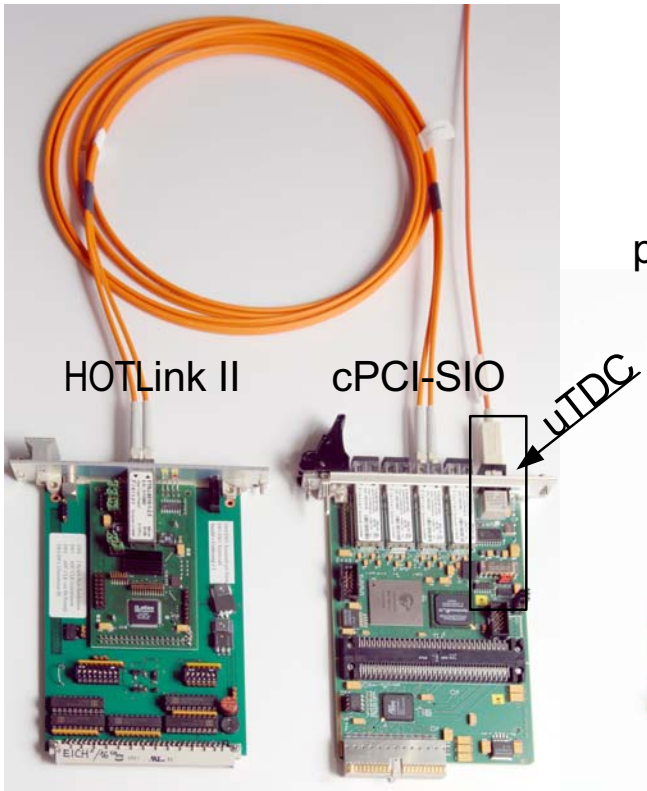
4 incoming data streams

Time Stamped DAQ

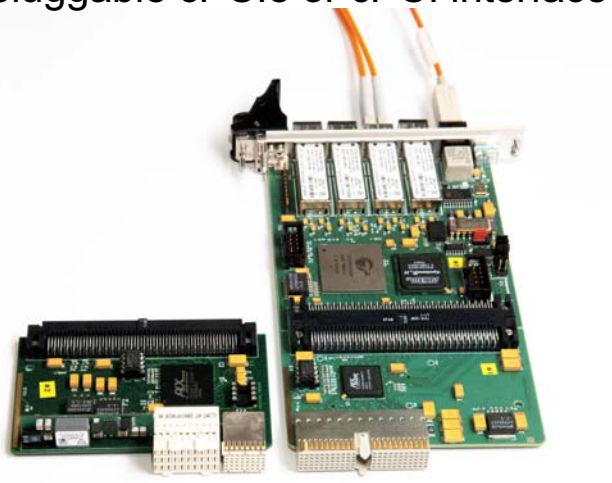
Fast Bolometry ADC Pipeline with cPCI-SIO & SUN



Yellow Card + SIOboard cPCIexpress or cPCI



pluggable cPCIe or cPCI interface



Zusammenfassung und Ausblick

Wir glauben mit der SIO Karte und der Pipeline-Backplane haben wir eine Konzept, das unsere Anforderungen für eine maßgeschneiderte Echtzeit-DAQ erfüllt.

1. Echtzeitfähig mit extrem kurzer Latenzzeit und zentral synchronisierter Zeitbasis
2. Hohe Datenaufnahmeraten durch DMA, Nutzung des billigen Rechnerspeichers
3. Flexible Anpassbarkeit der Peripherie an besondere Erfordernisse des Experiments
4. Stabiles multi-platform Rechnerinterface mit einfachen Schnittstellen
5. Kopplung von Diagnostik, Analyse & Steuerung im schnellen Netzwerkverbund

Wir arbeiten gerade an Diagnostiken, die bis zu 700 MB/s aufzeichnen sollen.

Wir arbeiten aber auch an der Kopplung solcher Diagnostiken mit Modellrechnungen, die in Echtzeit ein Physik-Modell auf der Basis der gemessenen Daten berechnen, um daraus am Ende in der schnellen Steuerung Regelungsgrößen abzuleiten.

Wir würden uns freuen,
wenn andere Arbeitsgruppen und Experimente
dieses Konzept interessant finden würden.

in der Diskussion gestellte Fragen

- (???) Kann man bei zwei verschiedenen Diagnostiken gleichzeitig eine Messung auslösen?
  - (Behler) Ja, die Counter in beiden Diagnostiken laufen synchronisiert auf gleichem Zählerstand, der die Zeit repräsentiert. Wenn man den Komparator in beiden Systemen mit einem Zählerstand läd, der in der Zukunft liegt, werden bei geeigneter Programmierung der Triggerlogik in beiden Systemen gleichzeitig Samplingtrigger erzeugt und gleichzeitig Daten aufgezeichnet.
- (???) Wenn man die Modellrechnungen in die Vorstufen legt, dann könnte man nur die berechneten Daten als komprimierten Strom schicken und so den Datenstrom wesentlich reduzieren. Eine Rekonstruktion der gemessenen Daten wäre durch eine inverse Anwendung des Modells möglich. ?
  Im Prinzip ist das zutreffend und man könnte solche Modellrechnungen z.B. in Prozessoren auf den Eingangskanälen unterbringen. Die Implementierung von Eingangskarten mit FPGA ist auch bereits angedacht. Aber es gibt mehrere Gründe, die gegen dieses Verfahren sprechen:
  - (Behler) Die Modelle können sehr groß sein. Es existiert z.B. ein 25000 Zeilen Fortran Code, dessen Portierung nach Labview zur Zeit geprüft wird.
  - (Raupp) Wir geben ziemlich viel Geld für den Betrieb eines so großen Experiments aus. Meistens kann man nicht vorausahnen, welche Effekte man sucht. Die unwiederbringliche Reduktion von Daten durch die Anwendung von Modellvorstellungen, die ja falsch sein können, ist unseren Anwendern nicht geheurer. Auch den Geldgebern gegenüber wäre es nicht zu rechtfertigen, an diesem Ende zu sparen.
  - (eine weitere mögliche Antwort, die aber in der Kürze nicht gegeben wurde) Die meisten Modelle, die hier in Betracht kommen, erlauben keine eindeutige Inversion der Berechnung, damit ist eine Rekonstruktion der Originaldaten unmöglich. Ebenso erfodern die meisten Modelle Daten von mehreren Diagnostiken. Diese Daten liegen aber auf der Erfassungsstufe nicht vor. Erst in der Analysestufe können diese Daten durch Kommunikation zwischen den verschiedenen Echtzeitdiagnostiksystem zusammengeführt werden. Aus Folie 3 kann man das beispielhaft sehen: MAX misst die Magnetfelder im Außenbereich, damit kann ein Flußflächensystem des Plasmas berechnet werden, das am Rand sehr gut ist und zur Mitte hin immer schlechter wird. MSX misst das Profil des Stroms im Plasma. Das Stromprofil kann zu einer verbesserten Berechnung der Flußflächen im Plasmainneren herangezzogen werden. Ein zweites Beispiel: ECE und MIR messen unabhängig voneinander Signale, die zur Lokalisation von Instabilitäten dienen können. Erst eine Korrelationsanalyse auf höherer Ebene über einen im Vergleich zur Einzelmessung längeren Zeitraum erlaubt eine eindeutige Bestimmung der Moden. Die Erfassung einiger MIR Signale durch ECE wäre möglich und ist tatsächlich geplant. Die Korrelation zwischen den verschiedenen Kanälen kann jedoch nicht im Front-End berechnet werden, sondern nur, wenn alle Signale der Diagnostik über einen Zeitraum von ca. 1000 Samples mit einander in Bezug gesetzt werden können.
  - (eine weitere mögliche Antwort, die ebenfalls nicht gegeben wurde) Es widerspricht der Anforderung nach Einfachheit und schneller Erlernbarkeit, wenn die Variation eines physikalischen Modells nicht vom Physiker selbst (Doktorand, Diplomand, Student) in einem Hochsprachenmodell vorgenommen werden kann, sondern durch komplexe Programmierschritte für einen Spezialprozessor in einer stark eingeschränkten Umgebung (kein Netzwerk, etc.) aufbereitet werden muss.

Kritikpunkte (zur evtl. Diskussion)

- keine „klassische“ externe Triggermöglichkeit ✓ (so gewollt)
- nur einheitliche Samplingraten innerhalb einer SIO Gruppe ✓ (dito)
- Zusatzaufwand für Zeitvektor
  - Datenmenge
  - Transfer, Speicherbelastung
  - erhöhter Programmieraufwand
  - erhöhter Rechenaufwand

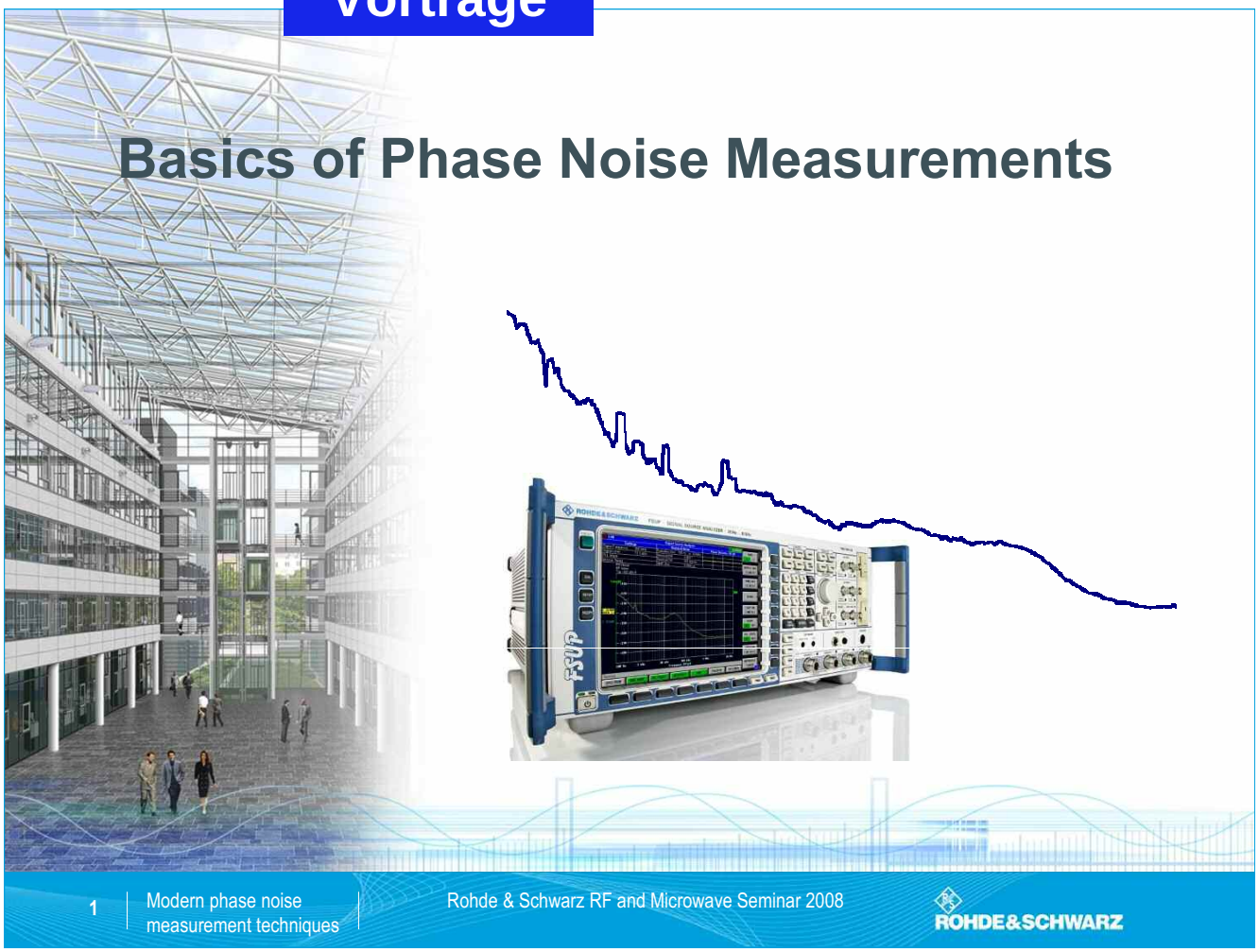
✓ (Bandbreite ausreichend, Kompression möglich)

✓ (gerechtfertigt)

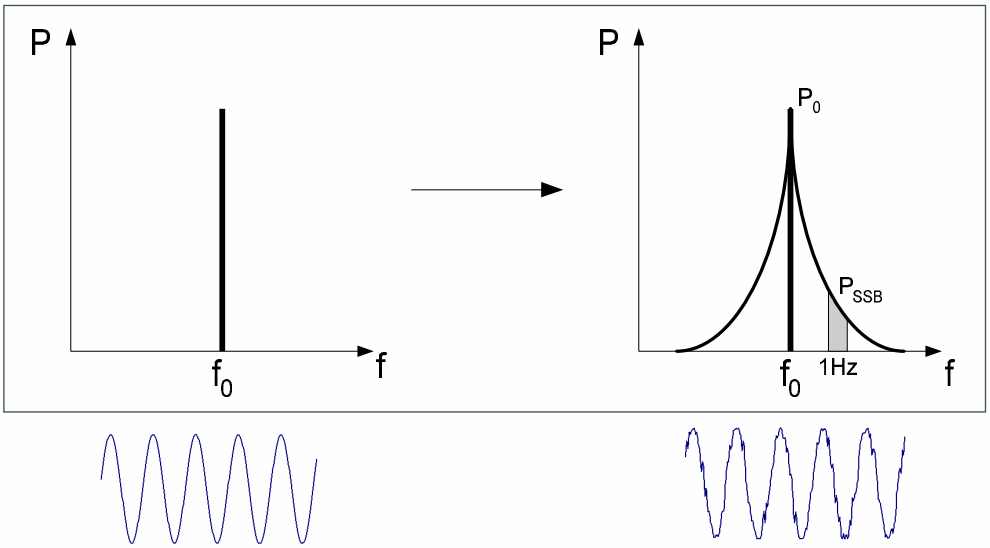
Publikationen der AUG CODAC Gruppe zur Thematik

- K. Behler, H. Blank, H. Eixenberger, A. Lohs, K. Lüddecke1), R. Merkel, G. Raupp, G. Schramm, W. Treutterer, M. Zilker, ASDEX Upgrade Team, Real-Time Diagnostics at ASDEX Upgrade - Architecture and Operation, Fusion Engineering and Design, **83** (2008) 304-311
- W. Treutterer, K. Behler, L. Giannone, N. Hicks, A. Manini, M. Maraschek, G. Raupp, M. Reich, A.C.C. Sips, J. Stober, W. Suttrop, ASDEX Upgrade Team, Real-Time Diagnostics at ASDEX Upgrade-Integration with MHD Feedback Control, Fusion Engineering and Design, **83** (2008) 300-303
- G. Raupp, K. Behler, R. Cole, K. Engelhardt, A. Lohs, K. Lüddecke, W. Treutterer, G. Neu, T. Vijverberg, D. Zasche, Th. Zehetbauer, ASDEX Upgrade Team, Real-Time Control and Data Acquisition with ASDEX Upgrade's New Time System, Fusion Engineering and Design, **81** (2005) 1747-1751
- A. Lohs, K. Behler, K. Lüddecke, G. Raupp, ASDEX Upgrade Team, The ASDEX Upgrade UTDC and DIO cards - a family of PCI/cPCI devices for rea, Fusion Engineering and Design, **81** (2006) 1859-1862
- G. Raupp, K. Behler, R. Cole, K. Engelhardt, A. Lohs, K. Lüddecke, G. Neu, W. Treutterer, Th. Vijverberg, D. Zasche, Th. Zehetbauer and ASDEX Upgrade Team, Replacement strategy for ASDEX Upgrade's new control and data acquisition, Fusion Engineering and Design, **71** (2004) 41-45
- Gerhard Raupp, R. Cole, K. Behler, M. Fitzek, P. Heimann, A. Lohs, K. Lüddecke, G. Neu, J. Schacht, W. Treutterer, D. Zasche, Th. Zehetbauer, M. Zilker, A "Universal Time" system for ASDEX Upgrade, Fusion Engineering and Design, **66-68** (2003) 947-951
- M. Zilker, P. Heimann, High-speed data acquisition with Solaris and Linux operating systems, Fusion Engineering and Design, **48** (2000) 193-197
- M. Zilker, K. Hallatschek, P. Heimann, F. Hertweck, ASDEX Upgrade Team, Multiprocessor systems for real-time data acquisition on the ASDEX Upgrade and future plasma experiments, Fusion Engineering and Design, **43** (1999) 417-423
- K. Behler, H. Blank, A. Buhler, R. Drube, H. Friedrich, K. Förster, K. Hallatschek, P. Heimann, F. Hertweck, J. Maier, R. Merkel, M. -G. Pacco-DÃŒchs, G. Raupp, H. Reuter, U. Schneider-Maxon, R. Tisma, M. Zilker, Review of the ASDEX Upgrade data acquisition environment - present operation and future requirements, Fusion Engineering and Design, **43** (1999) 247-258

Basics of Phase Noise Measurements

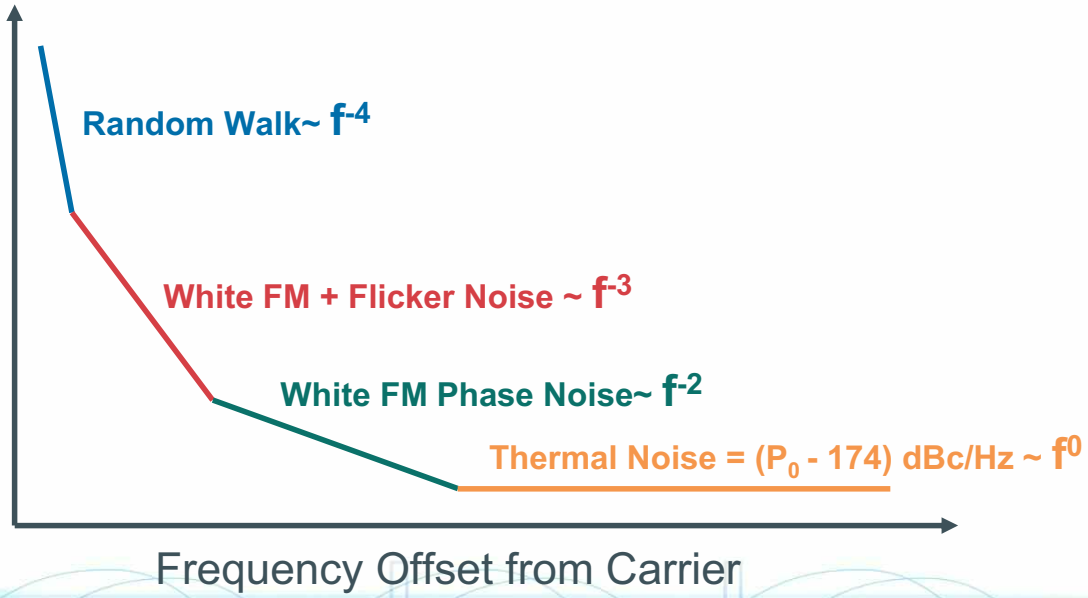


Phase Noise – What is this?

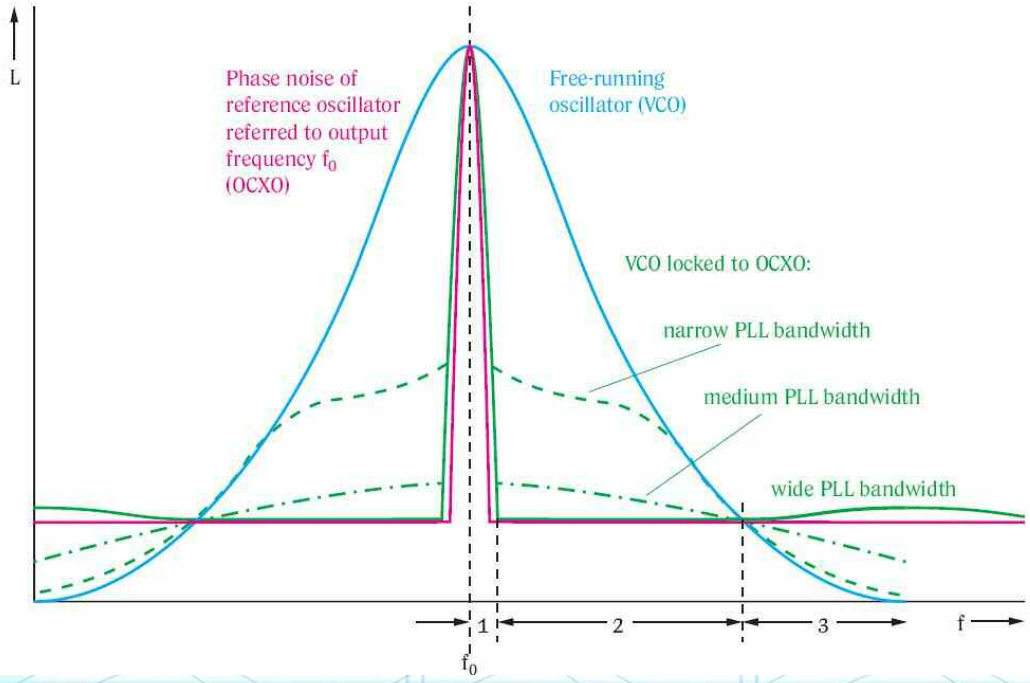


$$L(f_m) = 10\log\left(\frac{Single\_Sideband\_Power\_related\_to\_1Hz\_P_{SSB}}{Carrier\_Frequency\_Power\_P_0}\right) \quad [dBc(1Hz)]$$

Phase Noise – Typical Behavior of Oscillator Phase Noise

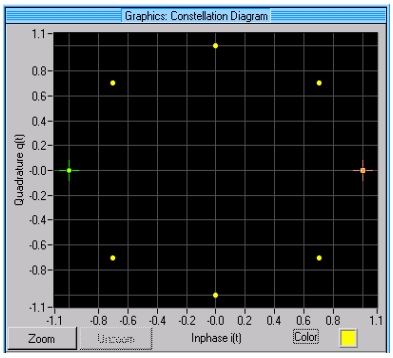


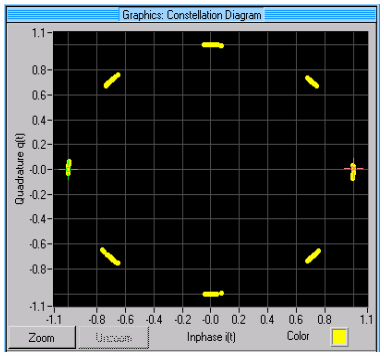
Phase Noise – of Locked Oscillators

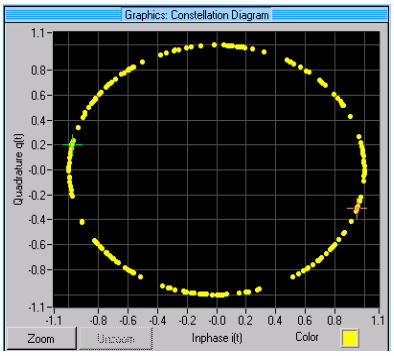


Digital Modulation

Impact of phase noise on modulation quality, e.g. 8PSK

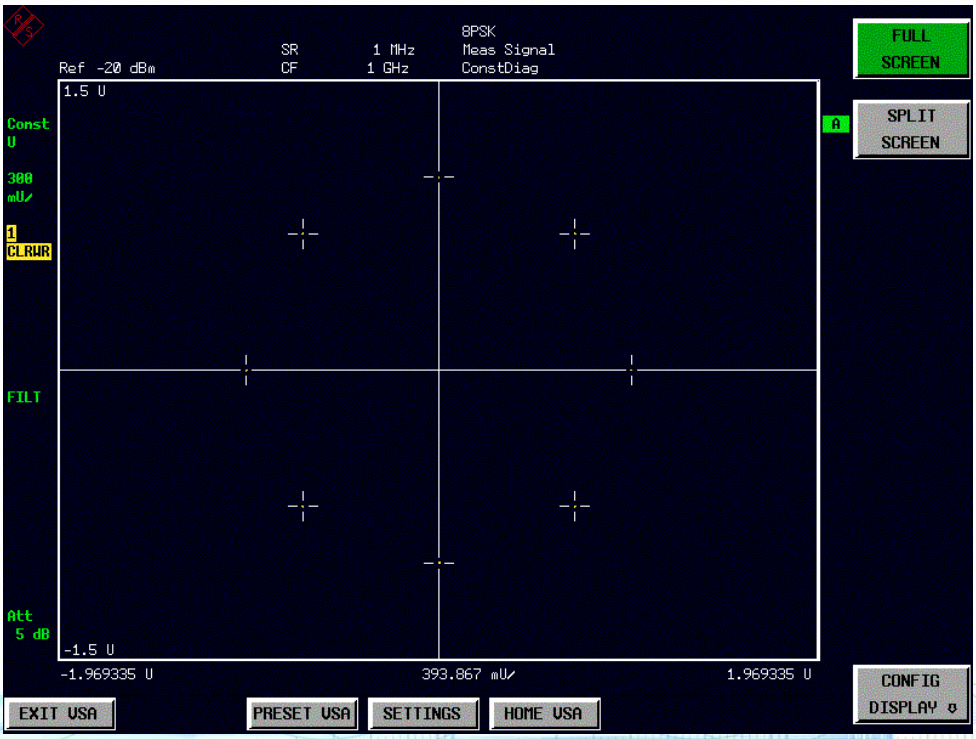




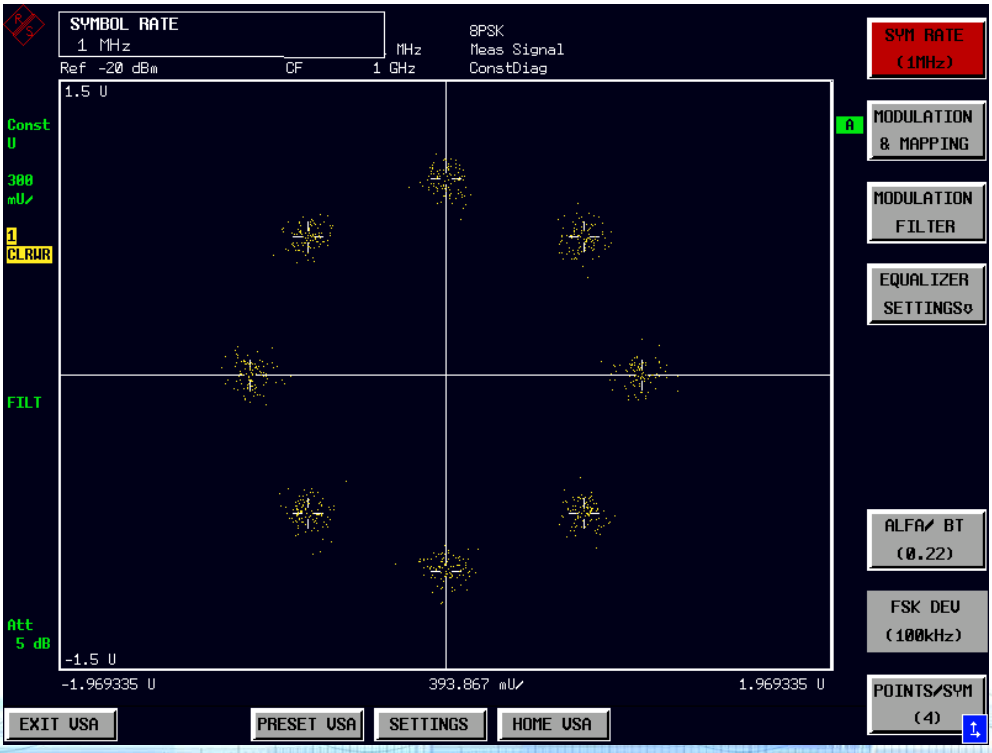


increasing phase noise

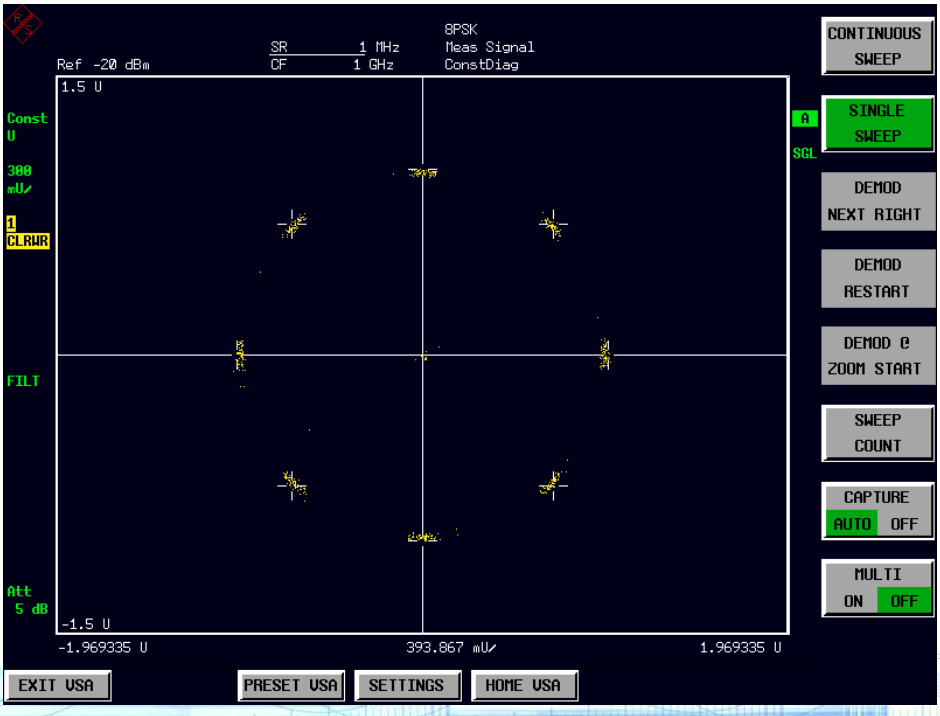
Ideal Source 8PSK Modulation



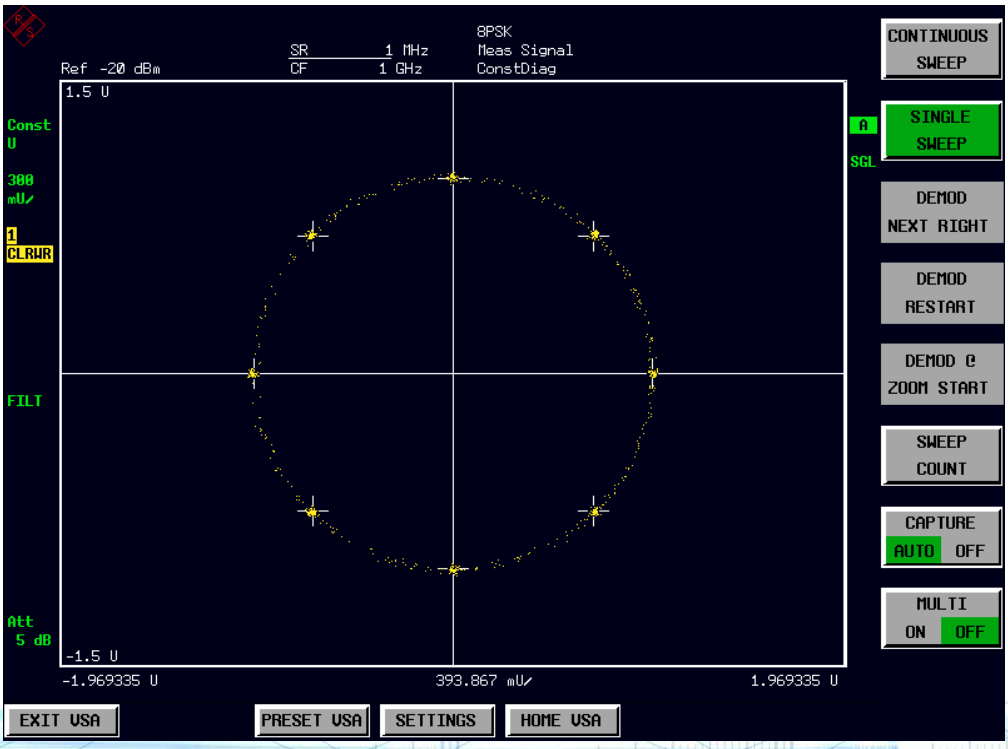
AM Noise and Phase Noise



Mainly Phase Noise – Weak Performance

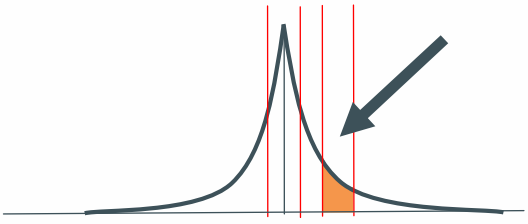


Mainly Phase Noise – Poor Performance



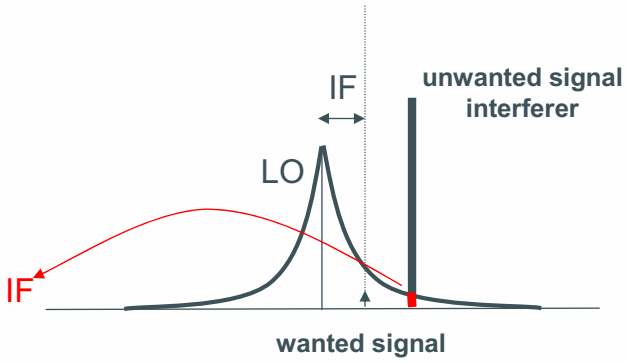
Phase Noise : Important Parameter in RF Technology

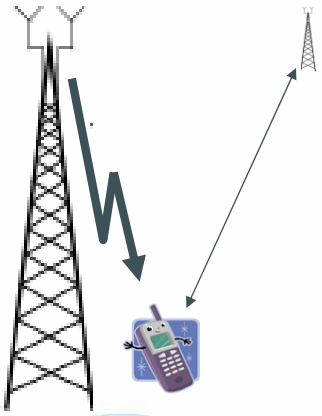
Adjacent Channel Power



Phase Noise : Important Parameter in RF Technology

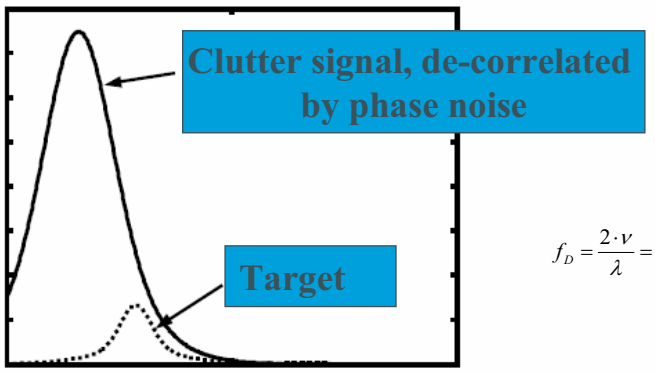
Sensitivity: Big interferer near the wanted signal





Phase Noise : Important Parameter in RF Technology

Radar Applications – Moving Target Indication



$$f_D = \frac{2 \cdot v}{\lambda} = \frac{2 \cdot 4\,km/h}{\left(\frac{3 \cdot 10^8 \frac{m}{s}}{10 \cdot 10^9\,Hz}\right)} = \frac{2 \cdot \frac{4 \cdot 10^3}{3600}\frac{m}{s} \cdot 10 \cdot 10^9 \frac{1}{s}}{3 \cdot 10^9 \frac{m}{s}} = 74Hz$$

Spectrum Analyzer Method

Direct Spectrum Analysis

1. Measurement of Carrier Level P_0
2. Measurement of (noise-) power at offset frequency f_m
3. Result:

$$L(f_m) = P_0 - (P_{noise,f_m} - 10 \cdot \log(\frac{B_{noise}}{Hz}) + D_{korr})$$

P_0: Carrier power

$P_{noise,fm}$: Noise at offset frequency f_m

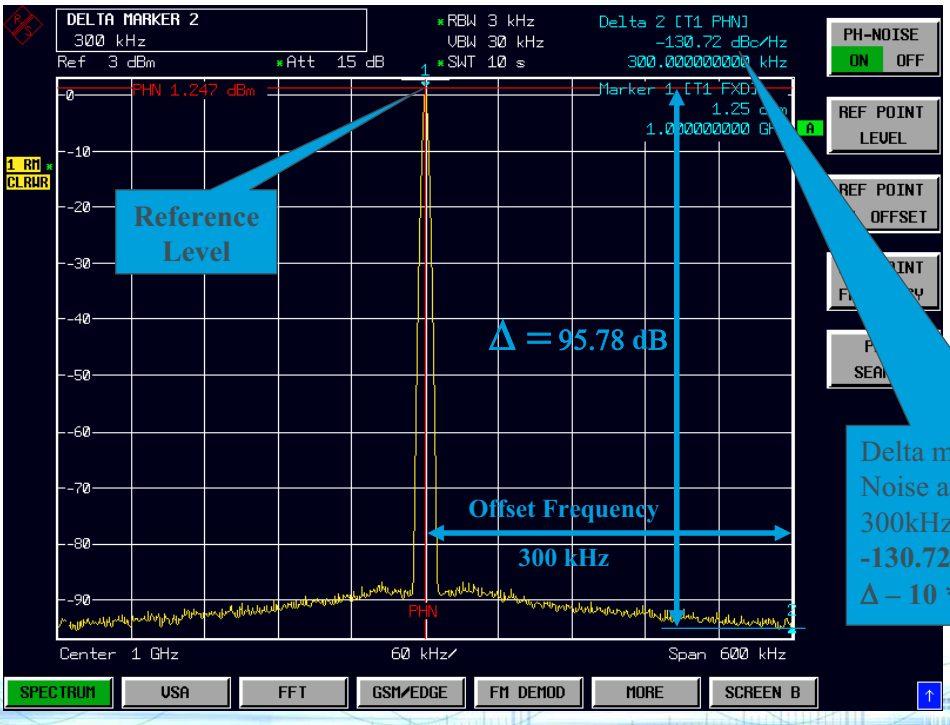
B_{noise}: Noise bandwidth of resolution filter

D_{corr}: RMS-detector (VBW > 3 · RBW, no Averaging): D_{corr} = 0 dB

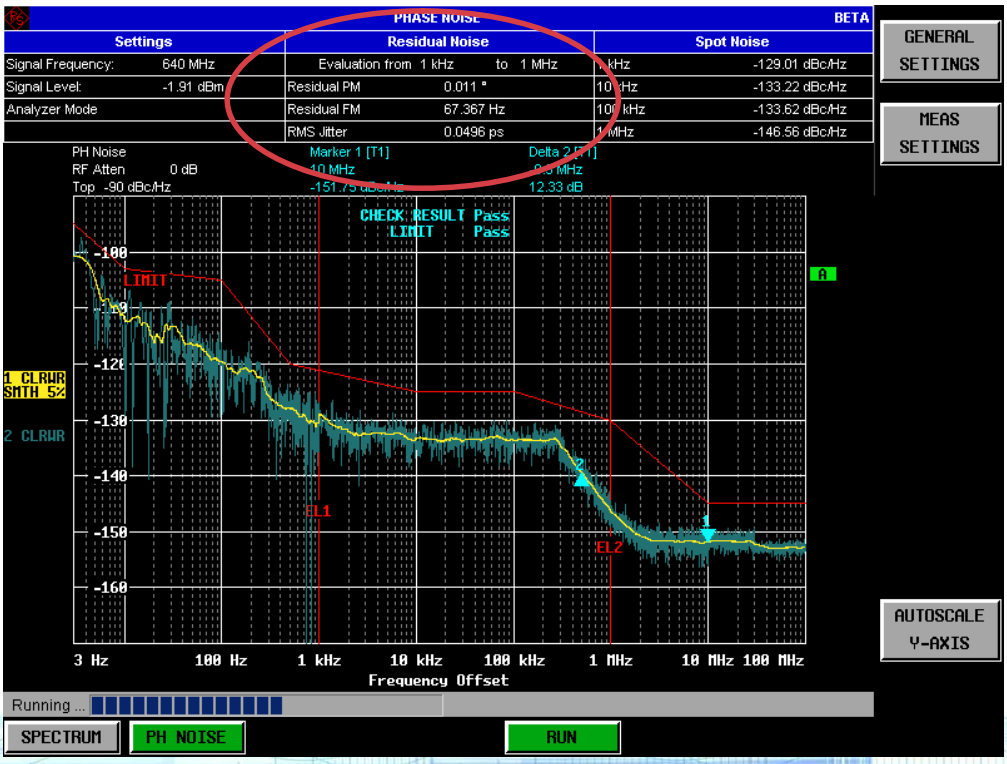
Sample-detector (VBW < RBW): D_{corr} = 2.5 dB

If the noise marker function of a spectrum analyzers is used, B_{noise} and D_{corr} are already compensated.

Spectrum Analyzer Method



Spectrum Analyzer Method



Residual Noise - Calculation

Phase noise is displayed as Single Side noise density L(f): $L(f) = 10 \cdot \log_{10}\left(\frac{S_\Theta(f)}{2}\right)$

where $S_\Theta(f)$ is the spectral density (W/Hz) of phase fluctuations

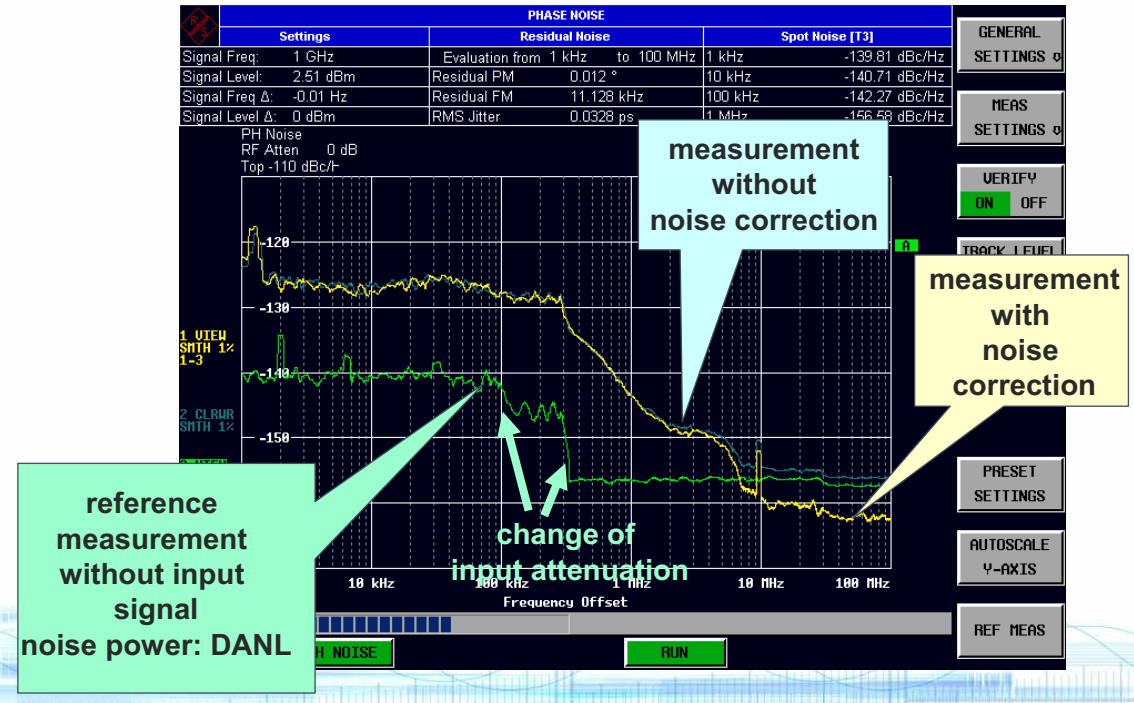
dBc/Hz -> W/Hz: $P_{norm}(f) = 10^{\frac{L(f)}{10}}$

Residual Phase Modulation $\Theta_{rms} = \sqrt{2\int_{f1}^{f2} P_{norm}(f)\,df}$

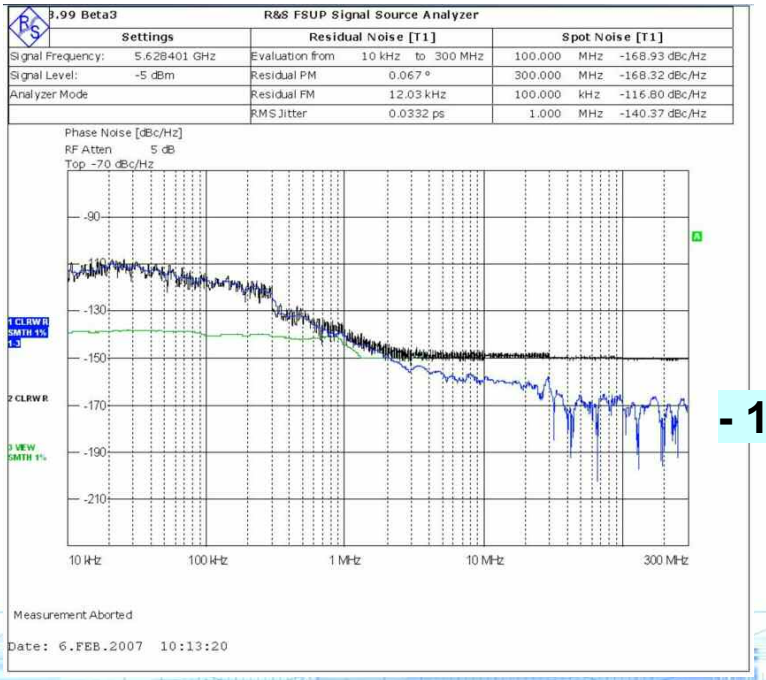
Residual Frequency Modulation $\Delta F_{rms} = \sqrt{2\int_{f1}^{f2} f^2 P_{norm}(f)\,df}$

Jitter $jitter_{rms} = \frac{\Theta_{rms}}{2\pi f_{osc}}$

Spectrum Analyzer Method with Noise Correction



Spectrum Analyzer Method with Noise Correction



- 170 dBc

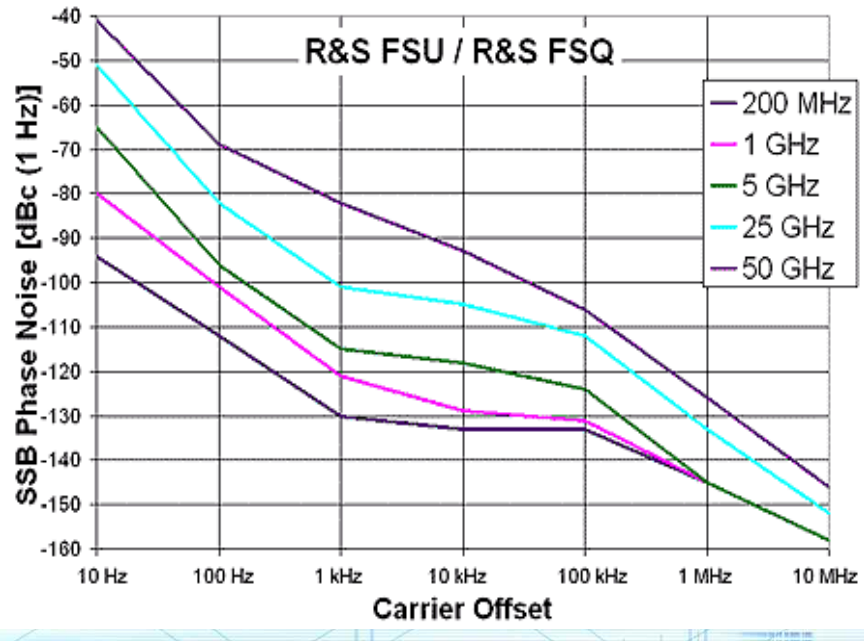
Advantages of the Spectrum Analyzer Method

- Easy and fast measurement setup
- High offset range (up to 1 GHz)
- A lot of additional functionality necessary for signal source characterization:
  - **Spurious emission measurements**
  - **Adjacent channel power leakage**
  - **Measurement of higher harmonics**
- Shows directly the phase noise, if AM noise is negligible

Disadvantages and Limitations of Spectrum Analyzer Method

- With spectrum analyzer method, AM noise and phase noise can not be distinguished
- Sensitivity is limited by inherent phase noise of the instrument

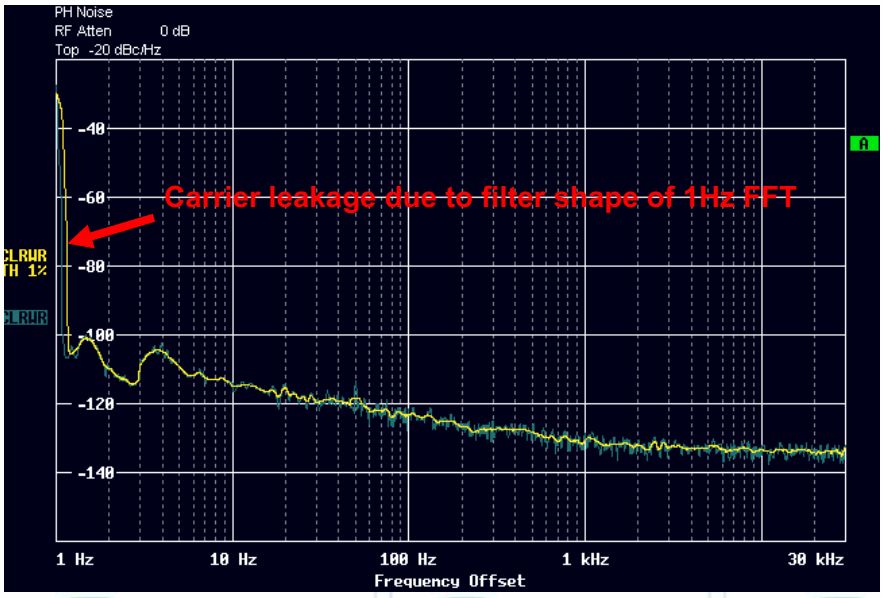
Disadvantages and Limitations of Spectrum Analyzer Method



Disadvantages and Limitations of Spectrum Analyzer Method

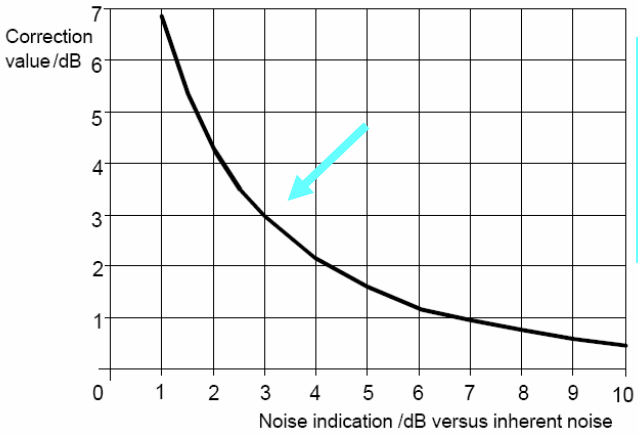
- With spectrum analyzer method, AM noise and phase noise can not be distinguished
- Sensitivity is limited by inherent phase noise of the instrument
- No carrier surpression
- At small offset frequencies the measurement range is limited by the minumum RBW and filter shape
- Restricted dynamic range

Disadvantages and Limitations of Spectrum Analyzer Method



Corrections and Error Calculation of Phase Noise Measurements

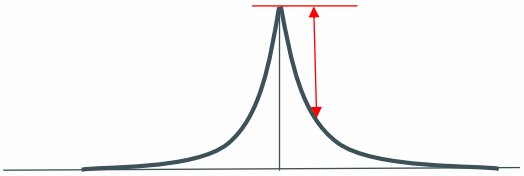
1. **Correction due to inherent phase noise of analyzer (comparison of measured value and specified value for R&S FSU/Q):**



Example:
If measured value is 3 dB enhanced compared to inherent noise, the measured phase noise of the DUT has to be corrected by 3 dB.

Corrections and Error Calculation of Phase Noise Measurements

2. **Linearity error of spectrum analyzer R&S FSU:**



3. **Uncertainty of reference level setting (if reference level has been changed during measurement):**

4. **Attenuator switching uncertainty (if attenuator has been changed during measurement):**

5. **Frequency response (at offsets > 100 kHz only):**

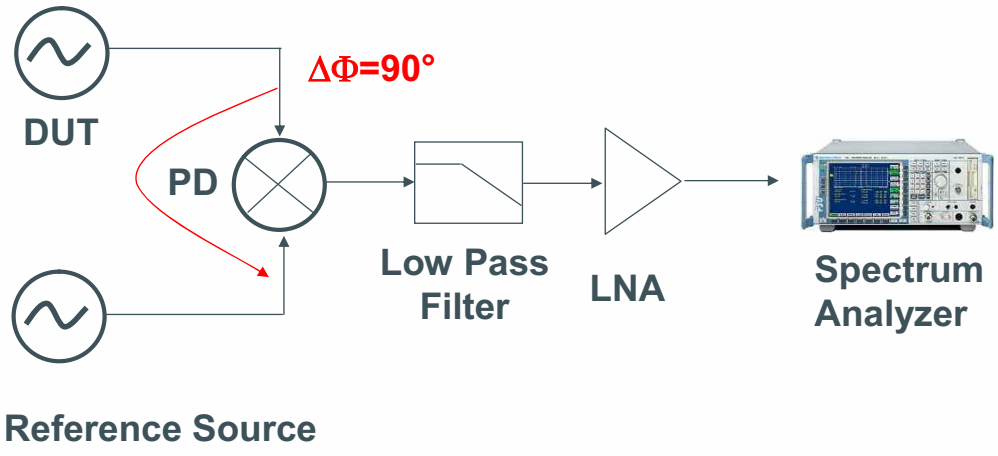
6. **Bandwidth uncertainty (due to calculation of dBc/Hz):**

Corrections and Error Calculation of Phase Noise Measurements

For accurate measurements a high end spectrum analyzer is necessary:

- **Excellent phase noise performance → 1**
- **Small linearity error due to digital back-end → 2**
- **High dynamic range (no switching of attenuators or change of reference level) → 3,4**
- **Low frequency response → 5**
- **Digital swept filters or FFT filters for small error of RBW → 6**

Phase Detector Method



Phase Detector Method

Input signals of the mixer (having 90° offset, i.e. in "Quadrature"):

$$U_L(t) = A_L \cdot \sin(2\pi f_L t + \Delta\varphi(t))$$
$$U_R(t) = A_R \cdot \cos(2\pi f_R t)$$

Output signals of the mixer:

$$U_{IF}(t) = K(A_R, A_L) \cdot \{\sin[2\pi(f_L - f_R)t + \Delta\varphi(t)] + \sin[2\pi(f_L + f_R)t + \Delta\varphi(t)]\}$$

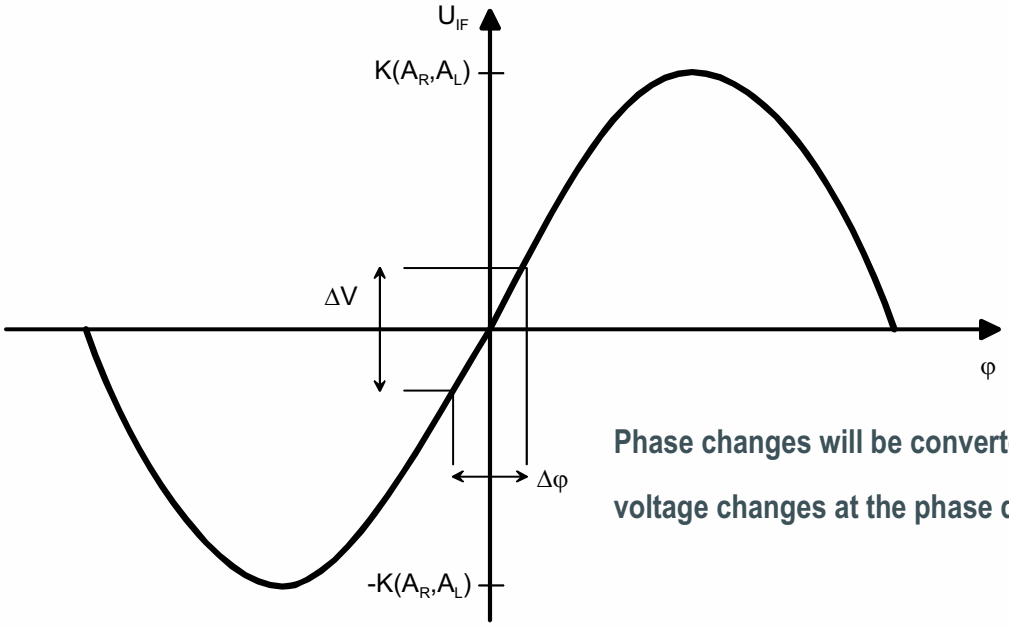
After low-pass filtering and assuming $f_L = f_R$ we get:

$$U_{IF}(t) = K(A_R, A_L) \cdot \sin[\Delta\varphi(t)]$$

For small changes in phase (simplification allowed for this kind of noise):

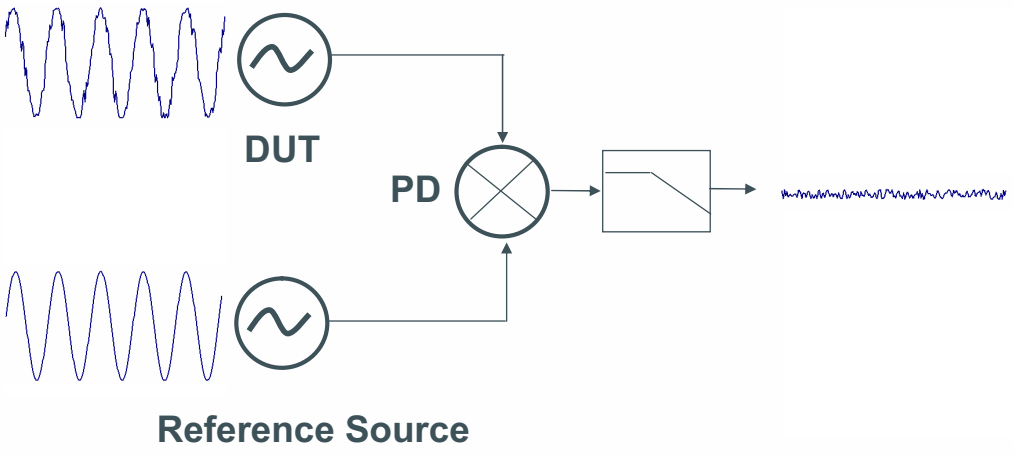
$$U_{IF}(t) \approx K(A_R, A_L) \cdot \Delta\varphi(t)$$

Phase Detector Method

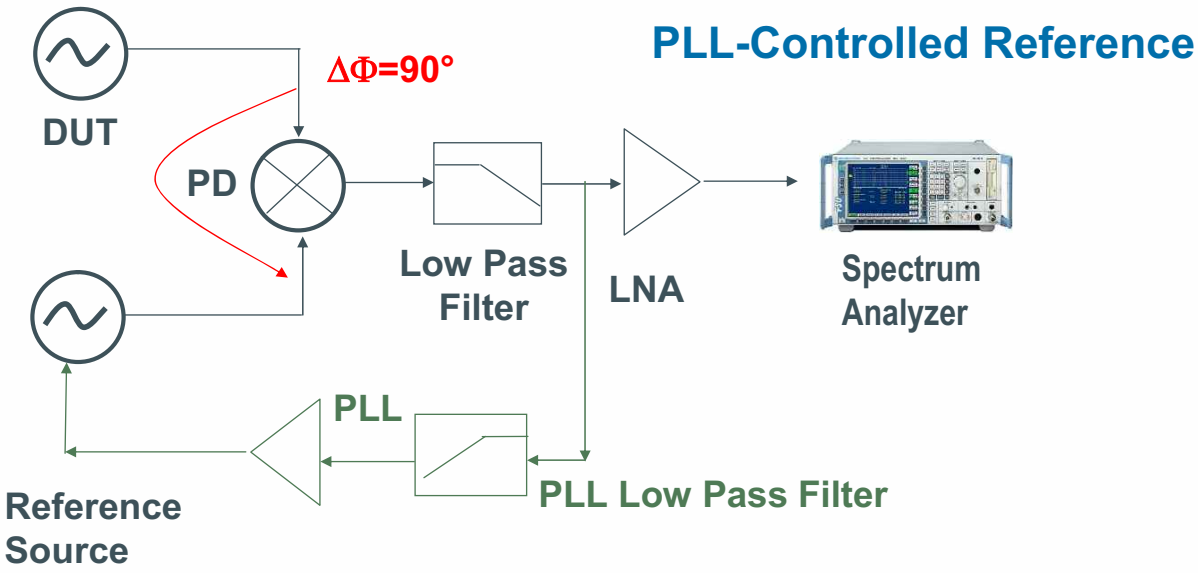


Phase changes will be converted to voltage changes at the phase detector

Phase Detector Method

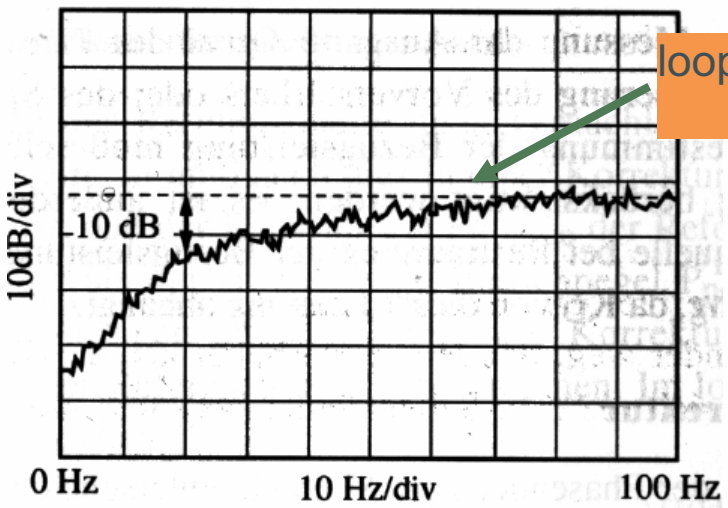


Phase Detector Method

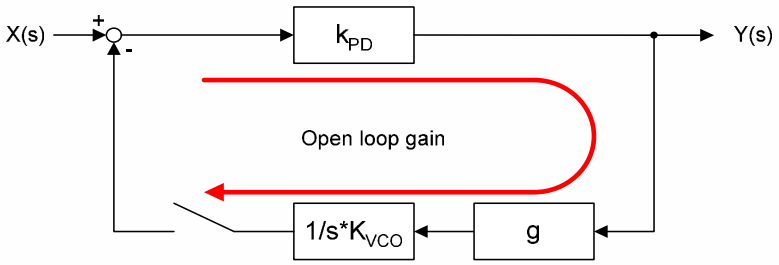


Phase Detector Method

Within the loop bandwidth the DUT phase noise is reduced



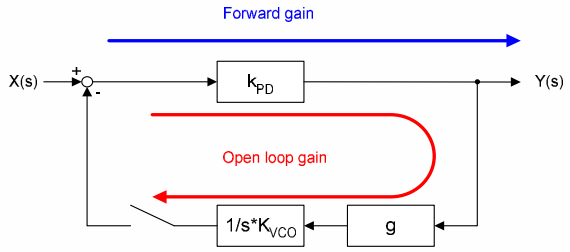
PLL Loop BW



$$LoopBW = k_{PD} \cdot K_{VCO} \cdot g_{Loop}$$

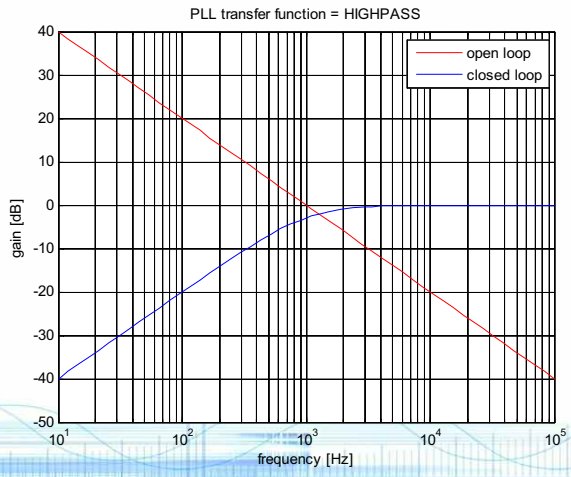
k_{pd}: phase detector slope
K_{VCO}: VCO tuning slope
g_{Loop}: loop gain
s: frequency $j\omega$

PLL Transfer Function



Example:

- k_{PD}=1V/rad
- K_{vco}=1MHz/V
- g=1/1000



Closed loop:

$$H_{CL}(j\omega) = \frac{\text{forward\_gain}}{1 + \text{open\_loop\_gain}} = \frac{k_{PD}}{1 + k_{PD} \cdot g \cdot \frac{k_{VCO}}{j\omega}} = k_{PD} \cdot \frac{j\omega}{j\omega + k_{PD} \cdot g \cdot k_{VCO}}$$

PLL Stability / Summary

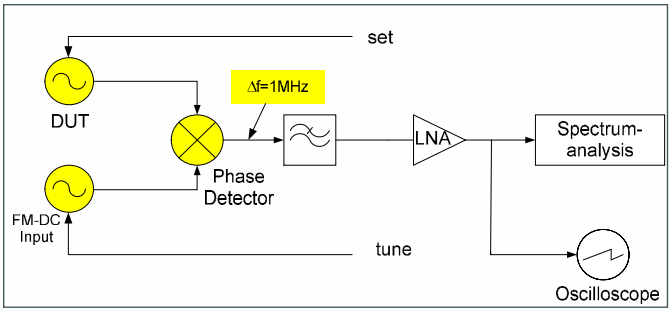
- The instrument must know all of the key parameters in order to calculate a stable PLL loop

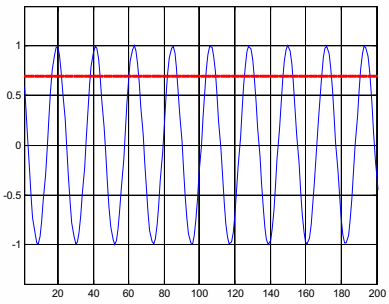
$$LoopBW[Hz] = k_{PD} \cdot K_{VCO} \cdot g_{Loop}$$

- PLL transfer function (Highpass) affects phase noise display.

$$H_{PLL}(s) = k_{PD} \cdot \frac{s}{s + k_{PD} \cdot g \cdot k_{VCO}}$$

Calibration – Beat Note

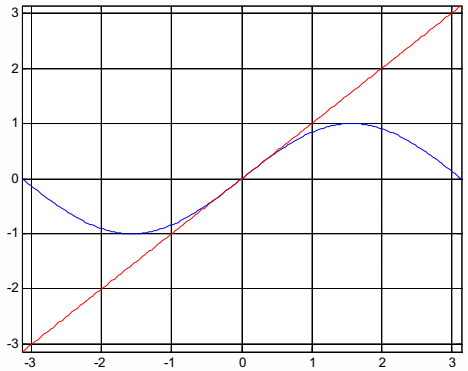




- offset frequency between reference and DUT is established
- ‚*beat note level*' is analyzed
- ‚beat note level' is the reference level for phase noise measurement (0 dBc)
- use beat note level in order to calculate k_{PD}

Phase Detector

$$U_{IF}(t) = k_{PD}(A_{REF}, A_{DUT}) \cdot \Delta\varphi(t)$$

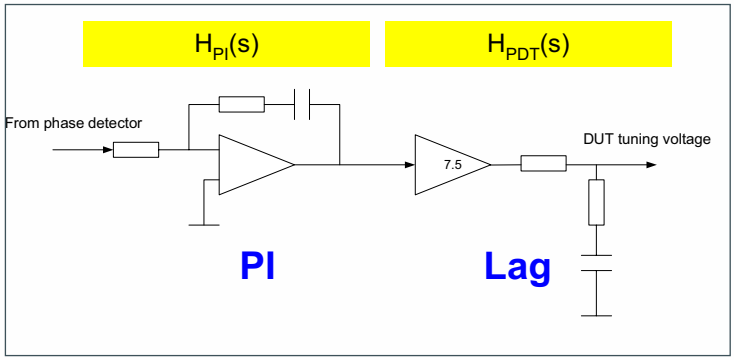


k_{PD} is:

the slope of the beat note curve at zero crosssing

$$k_{PD} = rms\_beat\_note\_voltage \cdot \sqrt{2}; \left[\frac{V}{rad}\right]$$

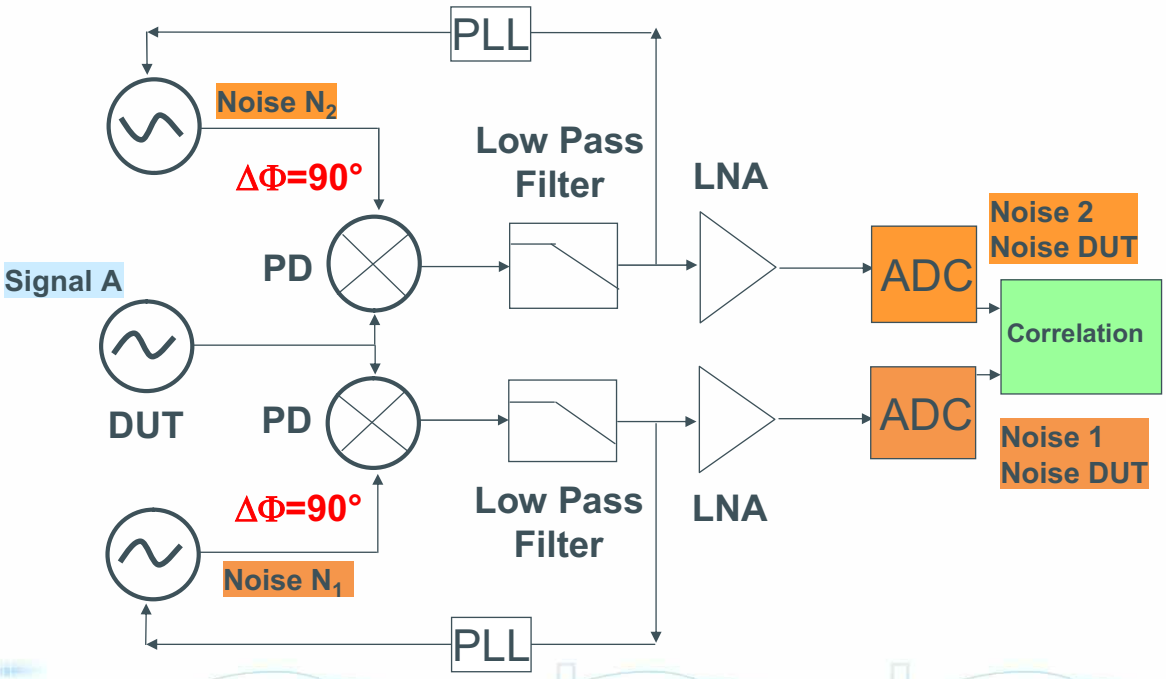
Loop Filter (DUT controlled)



$$H_{cl}(s) = \frac{Y(s)}{x(s)} = \frac{H_{PD}(s)}{1 + H_{PD}(s) \cdot H_{PI}(s) \cdot H_{PDT}(s) \cdot H_{VCO}(s)}$$

$$= \frac{k_{PD} \cdot T_I \cdot T \cdot s^3 + k_{PD} \cdot T_I \cdot s^2}{T_I \cdot T \cdot s^3 + \left(T_I + k_{PD} \cdot k_{\text{Feedback}} \cdot T_I \cdot T_D\right) \cdot s^2 + k_{PD} \cdot k_{\text{Feedback}} \cdot \left(T_I + T_D\right) \cdot s + k_{PD} \cdot k_{\text{Feedback}}}$$

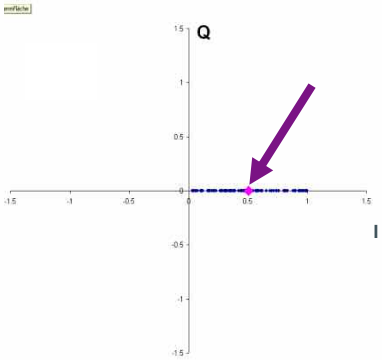
PLL Method with Cross-Correlation

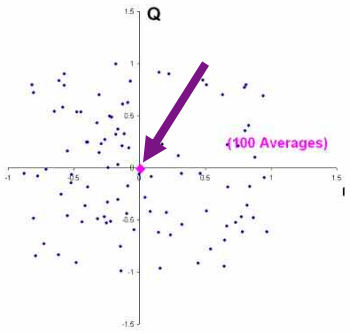


PLL Method with Cross-Correlation

$$L(f) \sim \left| \frac{1}{N} \sum_{i=1}^{N} (A_i + N_{1,i})(A_i + N_{2,i})^* \right|$$

$$L(f) \sim \left| \frac{1}{N} \sum_{i=1}^{N} A_i^2 + \underbrace{\frac{1}{N} \sum^{N} A_i N_{2,i}^*}_{\to 0} + \underbrace{\frac{1}{N} \sum^{N} A_i^* N_{2,i}}_{\to 0} + \underbrace{\frac{1}{N} \sum^{N} N_i N_{2,i}^*}_{\to 0} \right|$$





Advantage of PLL Method

- Carrier Suppression
  - Higher dynamic range for phase noise measurements at the spectrum analyzer (reference level ≠ carrier level)
  - Noise level of spectrum analyzer is of minor importance with optional LNA, which cannot be used in spectrum analyzer method due to restricted dynamic range

$$F = F_{LNA} + \frac{F_{spectrumanalyzer} - 1}{G_1}$$

  - Measurements at very small offsets are possible (no overlap of carrier with RBW filter due to filter shape)

Advantage of PLL Method

- AM Noise and Phase Noise clearly distinguishable:
  - No AM Noise at $\Delta\Phi = 90°$
    → only Phase Noise (30dB-40dB AM rejection)
  - No Phase Noise at $\Delta\Phi = 0°$
    → AM Noise (external test setup)
- It is possible to use an oscillator with very good phase noise performance as reference oscillator
- Two identical oscillators can be used
  (correction by 3 dB is necessary)

Advantage of PLL Method

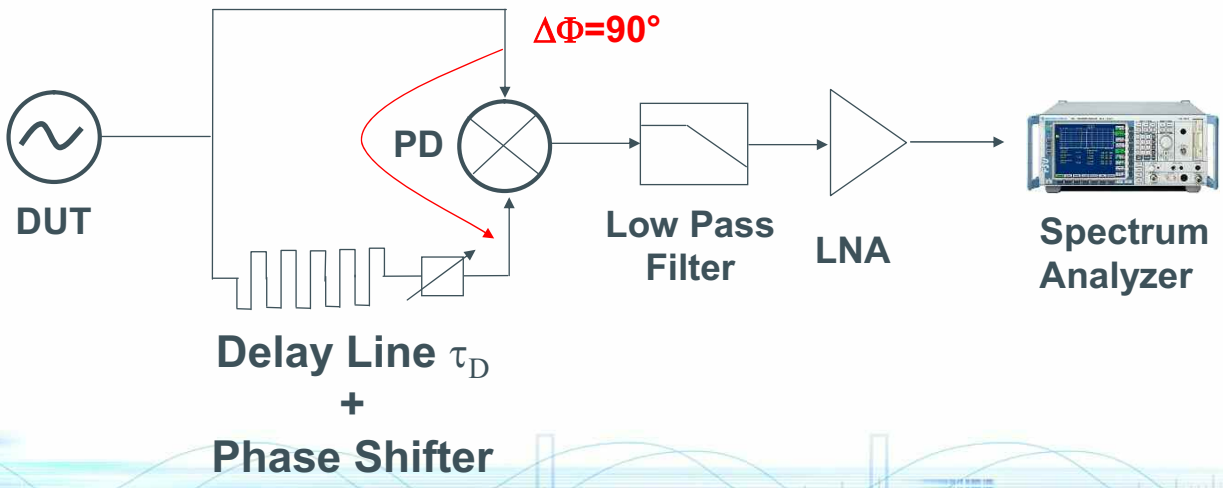
- **Cross Correlation Technique** can be used
  - The phase noise performance of the reference oscillators and test system can be **improved by up to 20 dB** through summation over 10000 measurements.

Disadvantage and Limitations of PLL Method

- Measurement setup is very complex
  - Calibration of measurements
  - Calculation of PLL parameters
- Restricted offset range
- Spectrum Analyzer is still necessary for measurement of:
  - Spurious Emissions
  - Higher Harmonics
  - Output Power
  - Adjacent Channel leakage power
  - ....

Delay Line Method

A broad band FM discriminator can be constructed by splitting the RF signal into two paths. One path is fed directly to the mixer the second path is passed through a delay line.



Delay Line Method

Advantage of Delay Line Method:

- No reference oscillator necessary
- Drift is not a problem any more
  - no synchronization necessary
- AM suppression
- Carrier suppression

sensitivity ~ τ_D^2
bandwidth: $1/\tau_D^2$
high bandwidth → small sensitivity

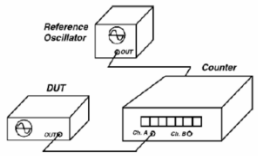
Disadvantage of Delay Line Method:

- restricted bandwidth f < $1/\tau_D$ due to due to sinx/x behavior
- high losses (small sensitivity) at high frequencies
- Calibration is necessary and more complicated

Allan Variance

The Allan variance is a measure for the **long-term stability** of an oscillator (e.g. stability of quartz oscillators), **not really a phase noise measurement method.**
The principal measurement setup consists of a spectrum analyzer with activated frequency counter.

- Measurement of the current frequency $\mathbf{f_k}$
- with a predefined measurement time τ
- Measurement is repeated M time



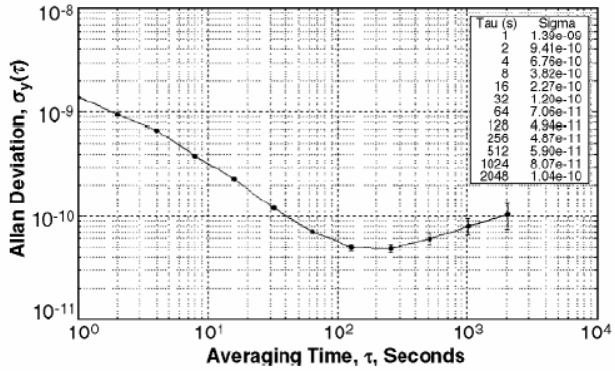
- The variance is then calculated with the following formula:

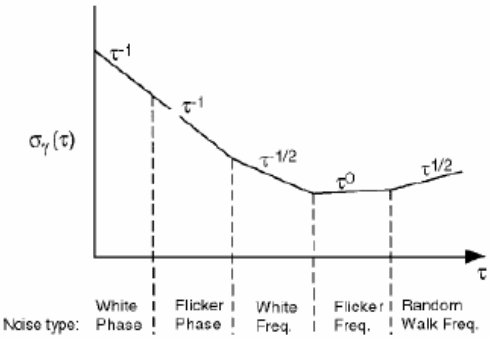
$$\sigma_{(M,2,\tau)} = \sqrt{\frac{1}{2(M-1)} \sum_{k-1}^{M-1} (f_{k+1} - f_k)^2}$$

Allan Variance

Stability of the device is improving, if averaging time τ gets longer, since some noise types can be removed by averaging.
The first type of noise to be removed by averaging is phase noise!

Main question:
How long do we have to measure until we get rid of noise of measurement system for characterizing long term stability?

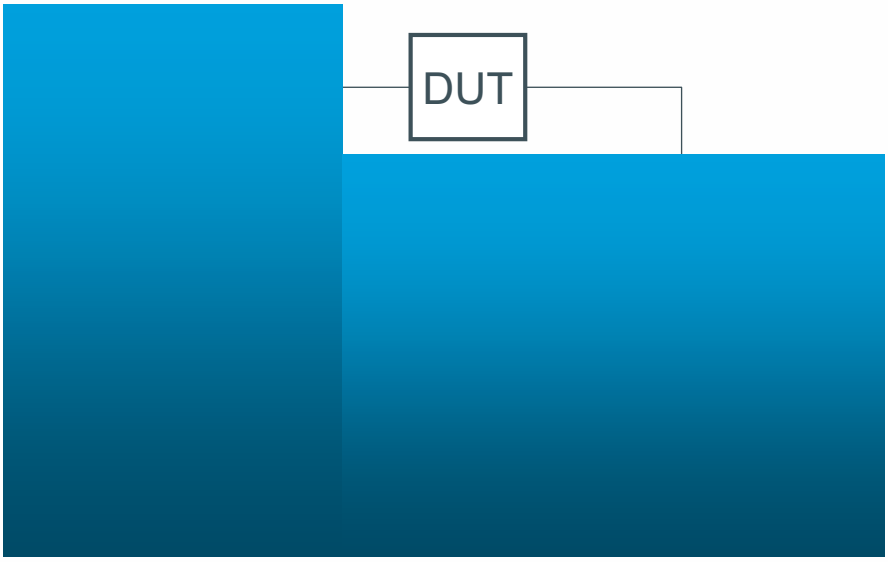




Comparison of Phase Noise Measurement Methods

Phase Noise measurement Method	Advantage	Disadvantage
Direct measurement with spectrum analyser: ○ FS-K40Phase ○ Noise Marker	• Easy setup / easy operation • No calibration necessary	• AM noise and phase noise cannot be seperated • No carrier suppression: - restricted dynamic range - overlap of RBW filter shape at low offset • Measurement accuracy limited by LO phase noise of spectrum analyzer
Phase Detector Method + PLL controlled reference	• AM noise and phase noise seperated • Carrier suppression - high dynamic range - small offsets • Noise of LO of SA of minor importance • Measurement of two identical oscillators posssible (3dB correction)	• Complicated setup • Calibration required • Very complicated calibration inbetween PLL bandwidth
+ Cross correlation method	• Improvement of phase noise of test system / reference oscillator (up to 20 dB)	• Longer measurement time for extremely low phase noise • Very complex setup
Delay line method	• Suitable for high drifting oscillators • No reference oscillator necessary • AM suppression • Carrier suppression (high dyn. range)	• Complicated setup • Complicated calibration • Restricted measurement range

Residual Noise of a two Port Device



Without DUT
no signal at the output
because of correlation
of the signals

Calibration is done
using the phase shifter

If frequency is converted by the DUT, two DUTs have to be measured and results have to be corrected by 3 dB.

AM Noise

AM noise becomes more and more important due to digital modulation schemes

Excerpt of a specification from a Philips IC:

UAA3587G

Low power GSM/GPRS multi-band transceiver

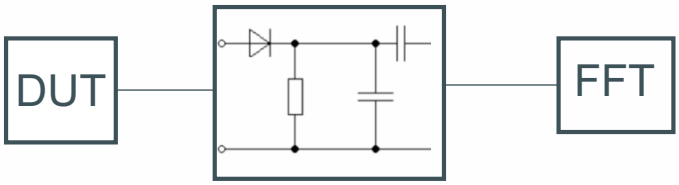
Rev.1.00 — 05 Jul 2005 Product Specification

$\Phi NOISE_{HB}$	phase noise output power density in DCS/PCS bands	Tamb=25°C; Δf = 400kHz; G1TX1=1; note 1	-	-118	-116	dBc/Hz
		Tamb=25°C; Δf = 1.8MHz; G1TX1=1; note 1	-	-130	-121	dBc/Hz
		Tamb=25°C; Δf = 20MHz; G1TX1=1; note 1	-	-	-154	dBc/Hz
$AM_{NOISE,LB}$	AM noise output power density in GSM850/900 bands	Tamb=25°C; Δf = 20MHz; G1TX1=0;	-	-170	-	dBc/Hz
$AM_{NOISE,HB}$	AM noise output power density in DCS/PCS bands	Tamb=25°C; Δf = 20MHz; G1TX1=1;	-	-162	-	dBc/Hz

AM Noise

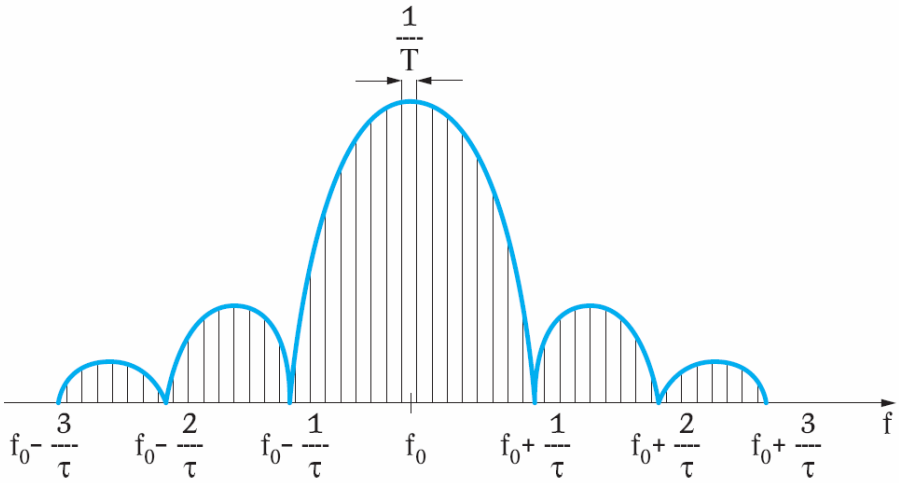
AM noise can be measured with a digital AM demodulator option:
- ❍ AM demodulation of input signal and calculation of the spectrum.
- ❍ Dynamic range (R&S spectrum analyzer): **max. 140 dBc**

For more dynamic range an external analog AM demodulator is required:
- ❍ 0° phase shift at phase comparator -> high DC offsets (sensitivity?)
- ❍ AM demodulation with diode

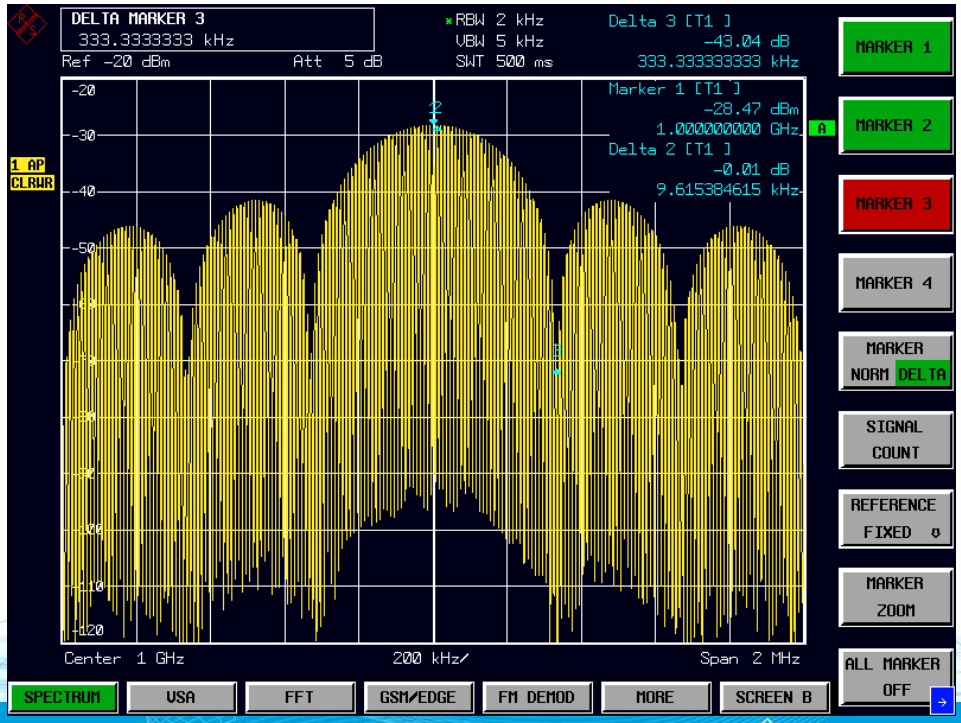


Pulsed Phase Noise Measurements

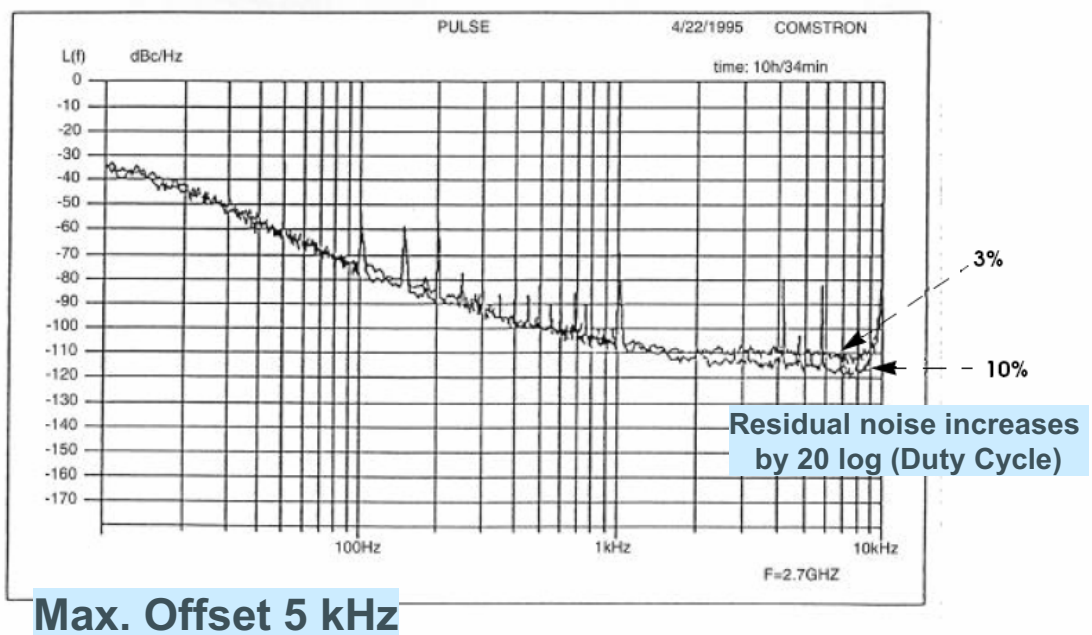
Pulsed Signal in Frequency Domain



Pulsed Phase Noise Measurements



Pulsed Phase Noise Measurements

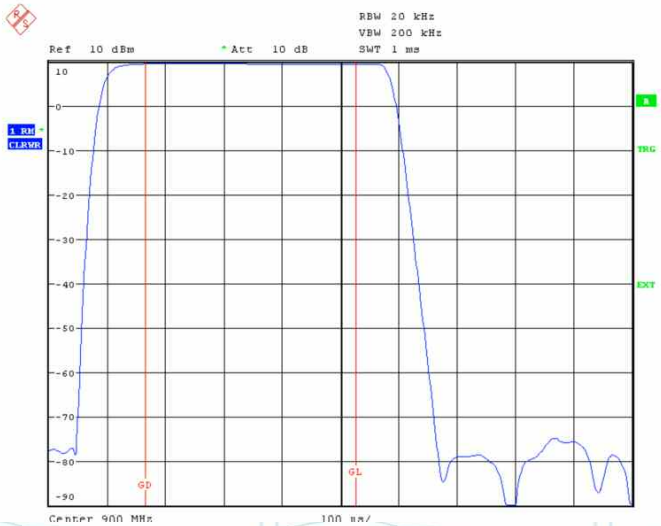


Max. Offset 5 kHz

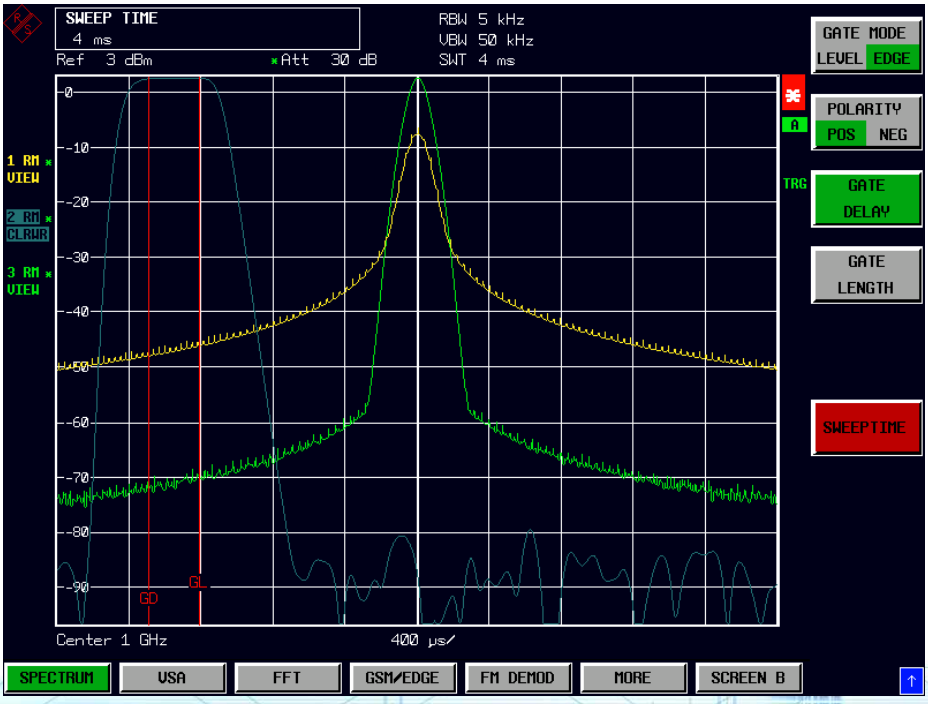
PRF:	10 kHz	Loop Bandwidth:	180 Hz
Duty Cycle:	3 and 10%	Tune Slope:	500 Hz
PRF Filter:	5 kHz	Gain:	70 dB

Pulsed Phase Noise Measurements

Gated Sweep with Spectrum Analyzer



Gated Sweep with Spectrum Analyzer



Typical Problems in VCO Design

- Does VCO cover the necessary frequency range, e.g. GSM?

Table 1-1 Downlink

P-GSM 900	935.2MHz	959.8MHz	FREQ
	1	124	ARFCN

VCO Tuning Characteristic

- What is the tuning sensitivity -> effective PLL design

VCO Tuning sensitivity

- What is the output power?

VCO RF power characteristic

- What is the suppression of higher harmonics?
  Can harmonics be used for IR mixer design?

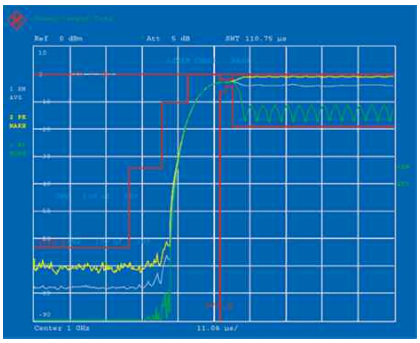
Harmonic power

- What happens when battery degrades

VCO Pushing ON

Typical Problems in VCO Design TDD systems

- Is settling time of VCO fast enough for TDD structure?
  Example: GSM-Burst:



Transient Measurements

- What happens when power amplifier is turned on?

VCO Pushing (voltage can drop down)

VCO Pulling (output impedance changes)

September 22, 2008

FPGAs von Xilinx: Technologien und Trends

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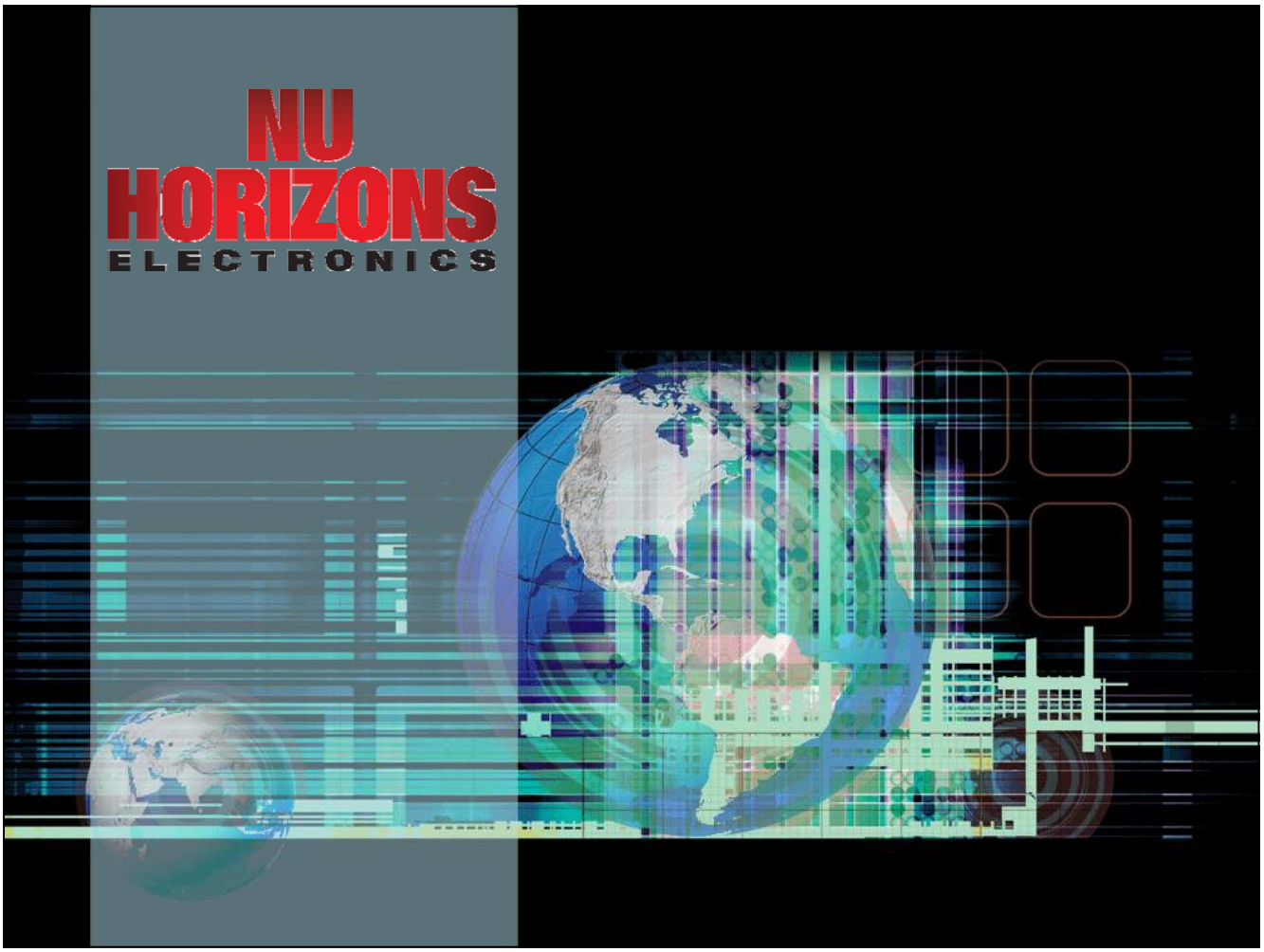

Why Programmable Solutions?

In today's competitive markets - programmability is "***Imperative***"

The Technologist's Dilemma

Changing Economics
Custom design is becoming more difficult and expensive

Changing Standards/Markets
Time-to-market and flexibility still highly valued

Rapidly increasing processing needs
Traditional solution are running out of gas

Xilinx is the Leading Provider of Programmable Solutions

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Agenda

- ***Foundation***
- ***Connectivity Solutions***
- ***Embedded Solutions***
- ***Signal Processing***
- ***Reference: Product Tables***

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Product Families & Target Applications

Ultimate System Integration with Risk-free Cost Reduction (EasyPath)

High-performance platform FPGAs optimized for highest-performance logic, connectivity, DSP & Embedded

Target Applications

Infrastructure Equipment, Wired & Wireless Communication

Lowest Total Cost… Period

Low-cost platform FPGAs optimized for lowest-cost system, logic, complex computation, and embedded processing

High Volume Consumer

Low-power, Low-cost Solutions for Mobile Applications

Ultra low power CPLDs with <20uA static and power mgmt

Low Power Handheld

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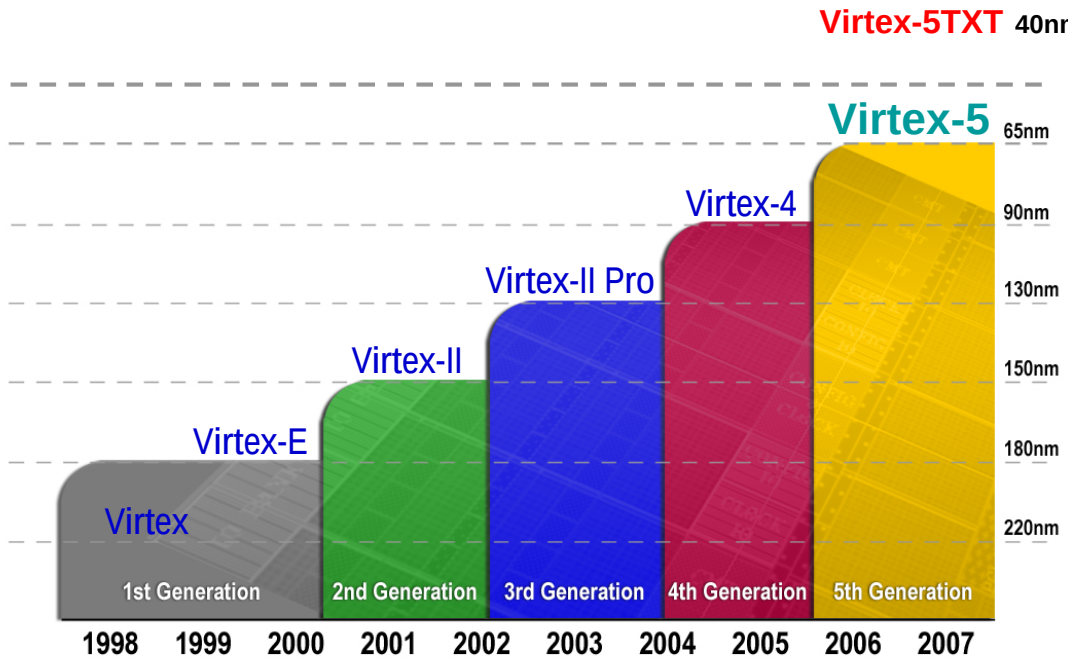
Virtex Product & Process Evolution



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Virtex-5 FPGA Family

The Ultimate System Integration Platform

65-nm platforms **40nm**

	LX	LXT	SXT	FXT	TXT
	High-performance logic	High-perf. logic w/ low-power serial I/Os	DSP and memory-intensive apps w/ low-power serial I/Os	Processing and memory-intensive apps w/ highest-speed serial I/Os	Double Transceiver Count Devices of FXT
	Logic	*Logic + Serial*	*DSP + Serial*	*Emb. + Serial*	*Emb. + Serial*
Logic					
On-chip RAM					
DSP Capabilities					
Parallel I/Os					
Serial I/Os					
PowerPC®					
In Production	*YES*	*YES*	*YES*	*Samples Now*	*Soon*

EasyPath low-risk, conversion-free cost reduction for all platforms: 30-75% cost savings

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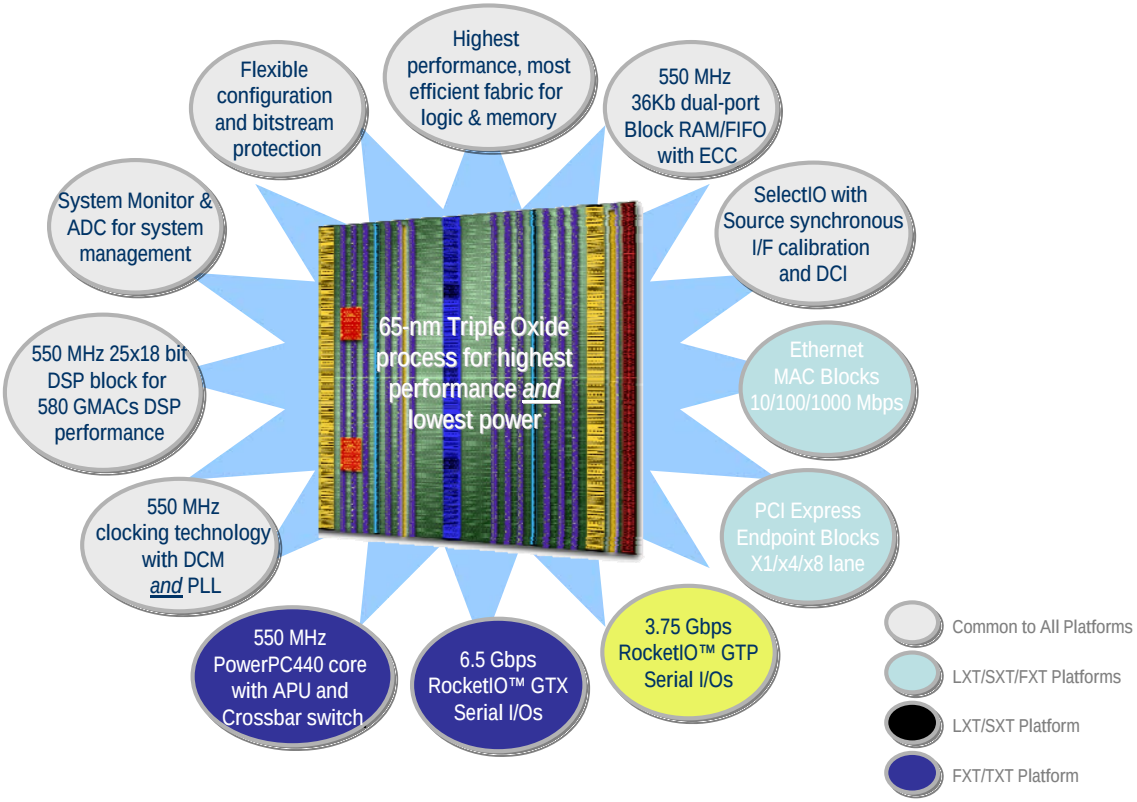
Virtex-5 Key Capabilities



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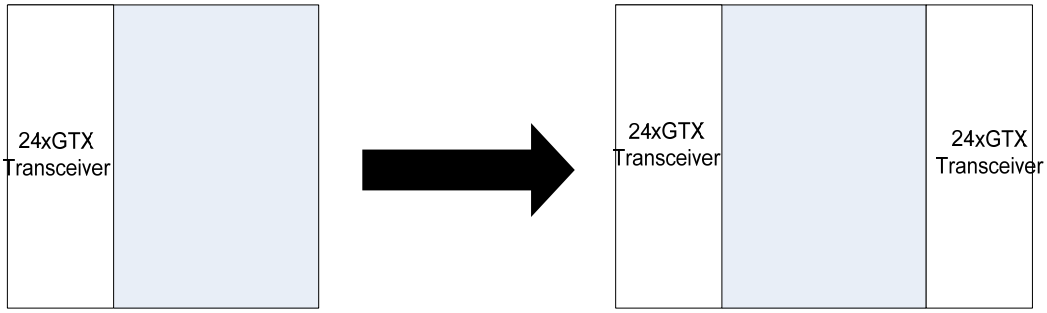
What is New in Virtex-5TXT

- Double Transceiver count device
- Most Applicable to the following markets:
  - Wired Communications
    - Wired Communications Customers who need
      - High-Throughput Line Cards (40Gbps, 100Gbps+)
      - Bridging Applications
      - Switching applications
  - Video and Medical Imaging
    - where high volumes of uncompressed video need to be piped around
- Faster
- Path to High Transceiver Counts than Competitive Solutions @ 40nm

V5TXT is an Extension of V5



- V5 FXT
  - 1 column of GTX 6.5G transceivers
  - Available for emulating the TXT
- V5 TXT
  - 2 columns of GTX 6.5G transceivers (same design, just an extra column)
  - Different mix of logic and BRAM (no changes to the column architecture, just a different mix)
- LOW RISK path to high transceiver counts using existing, proven transceiver architecture

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Virtex-5 TXT Platform

- Based on proven Virtex 5 FXT technology
  - Can test V5FXT SERDES (transceiver) today
- Two new high MGT count FPGAs
  - Transceivers counts: 40 & 48
  - Speeds: 6.5Gbps (FXT like)
  - Package migration in FF1759
- Tools Support
  - General Release ISE Service Pack 3: Sept'08

Virtex-5 TXT v4.40		TX150T	TX240T
CLB Y Array Size		200	240
CLB X Array Size		58	78
LUTs		92,800	149,760
Logic Cells		148,480	239,616
LUT RAM KBits		1,500	2,400
BRAM Blocks		228	324
BRAM KBits		8,208	11,664
CMTs		6	6
DSPs		80	96
GTX Channels		40	48
PCIe		1	1
EMACs		4	4
Package	Size		
FF1156	35	360,40	
FF1759	42.5	680,40	680,48

x,y | x = SelectIO Count, y = GTX Channel Count

UPDATE from previous slides
To improve memory performance

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Extended Spartan-3A Family

Lowest Total Cost ...

Lowest system cost

- Integrated features and only two power rails minimize external components
- Lowest static power and award winning power management modes
- Robust low-cost security

Cost-efficient logic design

- Largest selection of IP, reference designs, and I/O standards
- Non-volatile option provides largest integrated flash memory
- Seamless package migration to non-volatile devices

Low-cost complex computation and embedded processing

- Abundant set of DSP48A hard blocks speeds calculations and saves logic cells
- MicroBlaze 7 delivers inexpensive, highly functional Linux embedded processing

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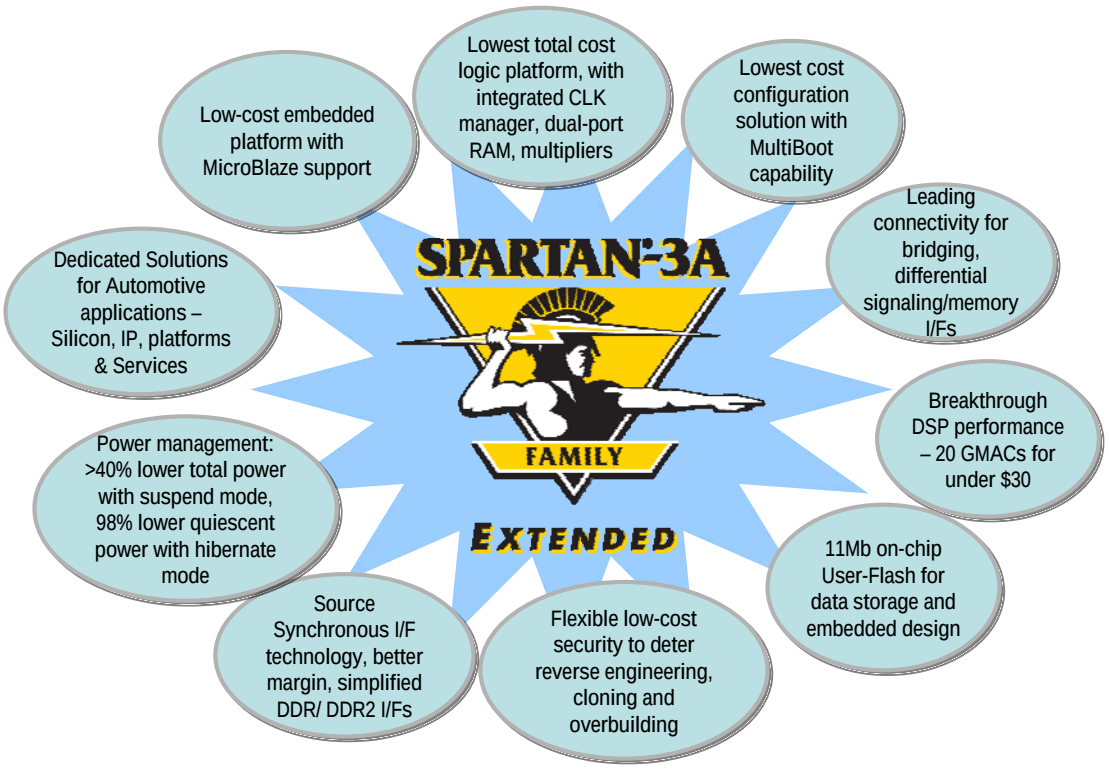
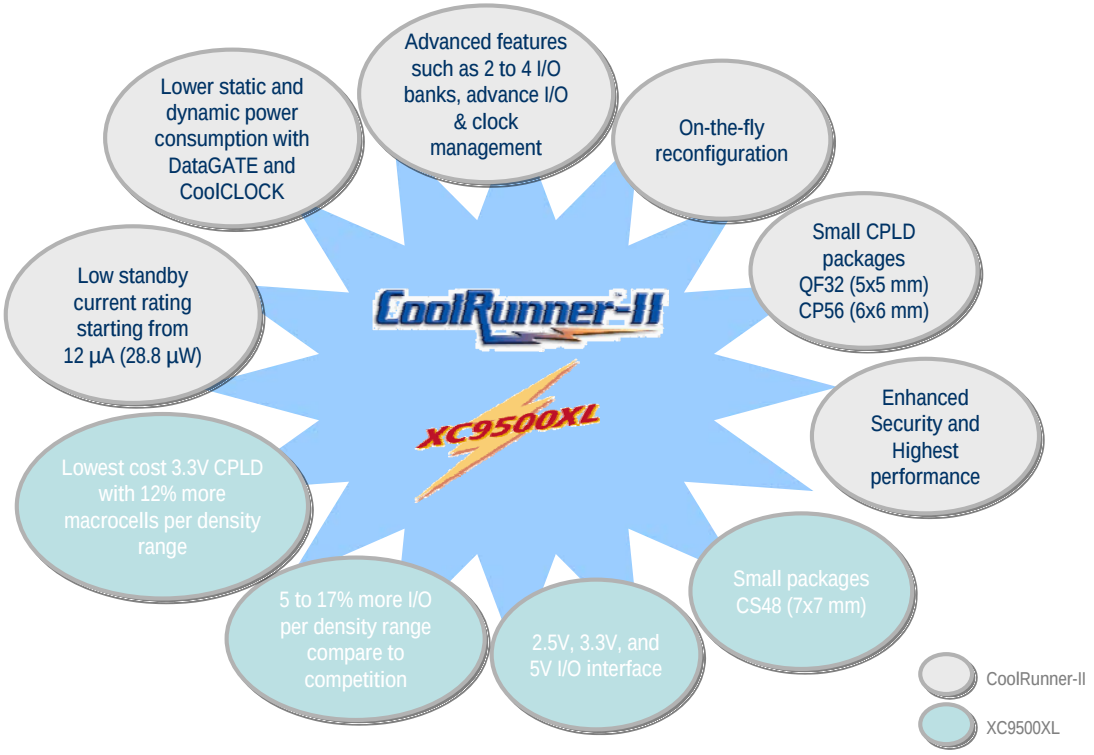
Spartan-3A Family Key Capabilities



Xilinx CPLD Key Capabilities



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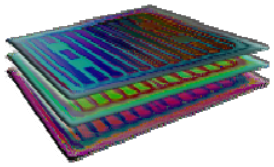
ISE™ Design Suite 10.1

One Environment for Logic, Embedded and DSP Design

Efficient logic implementation	Design analysis & planning	Interactive system debugging	Flexible embedded system design & programming	DSP system design (Simulink)	DSP algorithm development (MATLAB)
ISE Foundation	PlanAhead™	ChipScope™ Pro	EDK / Xilinx Platform Studio	System Generator	AccelDSP™

FPGA Implementation with ISE

Fast access to updates and evaluation



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ISE Key Capabilities

- **Easily meet timing budgets**
  - *SmartXplorer technology* – up to 38% higher performance
- **Simplify pin planning and ensure best place and route**
  - *PlanAhead tool* – design exploration and floor planning, on average 15% faster performance
- **Enable more "turns-per-day"**
  - *SmartCompile technology* – achieve performance goals in less time
  - 2X faster runtimes compared to previous version
- **Fast debug and verification in real-time**
  - *ChipScope Pro tool* – virtual logic analyzer inside the FPGA
- **Plus easier pin planning, power analysis and optimization**

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ISE WebPack vs. ISE Foundation

		ISE WebPACK	ISE Foundation
Platforms		Microsoft® Windows® XP Professional (32-bit) Microsoft Vista Business (32-bit) Red Hat Enterprise Linux 4 WS (32-bit) Red hat Enterprise Linux Enterprise 5 (32-bit) SUSE Linux Enterprise 10 (32 bit)	Microsoft Windows XP Professional (32/64-bit) Microsoft Vista Business (32/64-bit) Red Hat Enterprise Linux 4 WS (32/64-bit) Red Hat Enterprise Linux Desktop 5 (32/64-bit) SUSE Linux Enterprise 10 (32 and 64 bit))
Devices (FPGAs)	Virtex Series	**Virtex:** XCV50 - XCV600 **Virtex-E:** XCV50E - XCV600E **Virtex-II:** XC2V40 - XC2V500 **Virtex-II Pro:** XC2VP2 - XC2VP30 **Virtex-4:** **LX:** XC4VLX15, XC4VLX25 **SX:** XC4VSX25 **FX:** XC4VFX12 **Virtex-5:** **LX:** XC5VLX30, XC5VLX50 **LXT:** XC5VLX30T, XC5VLX50T **FXT:** XC5VFX30T **Virtex Q:** XQV100- XQV600 **Virtex QR:** XQVR300, XQVR600 **Virtex-E Q:** XQV600E	**Virtex:** All **Virtex-E:** All **Virtex-II/Pro:** All **Virtex-4:** **LX:** All **SX:** All **FX:** All **Virtex-5:** **LX:** All **LXT:** All **FXT:** All **Virtex Q/QR:** All **Virtex-E Q:** All
	Spartan Series	**Spartan-II/IIE:** All **Spartan-3:** XC3S50 - XC3S1500 **Spartan-3A:** All **Spartan-3AN:** All **Spartan-3A DSP:** XC3SD1800A **Spartan-3E:** All **Spartan-3L:** XC3S1000L, XC3S1500L **XA (Xilinx Automotive) Spartan-3:** All	**Spartan-II/IIE:** All **Spartan-3:** All **Spartan-3A:** All **Spartan-3AN:** All **Spartan-3A DSP:** All **Spartan-3E:** All **Spartan-3L:** All **XA (Xilinx Automotive) Spartan-3:** All
Devices (CPLDs)	CoolRunner™ XPLA3 CoolRunner-II CoolRunner-IIA XC9500 Series	All	

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Intellectual Property Cores

Augment Your Own R&D to Maximize Productivity and Reduce risk

Programmable hard IP
- Immersed in FPGA fabric
- Advantage over soft IP
  - 2x performance
  - 10x lower power
  - 10x less area

Customizable soft IP
- Built on FPGA fabric
- Examples
  - LogiCORE (from Xilinx)
  - AllianceCORE (from partners)
  - Reference Designs
- Advantage over hard IP
  - Most flexible
- Library of >400 blocks

Example IP for Virtex-5 Platform FPGAs

IP	Hard	Soft
Basic	BlockRAM/FIFO, System Monitor	BaseBlox, Memory I/Fs…
Connectivity	PHY (ser./par.), PCIe, GE, timing critical I/O logic & clocking	Serial and parallel I/F protocols…
Processing	PowerPC 440, Crossbar switch, DMA, MCI, Bus I/F	MicroBlaze, peripherals, accelerators…
DSP	XtremeDSP slice (MAC)	Algorithms, FEC…
System functions		Traffic Manager…

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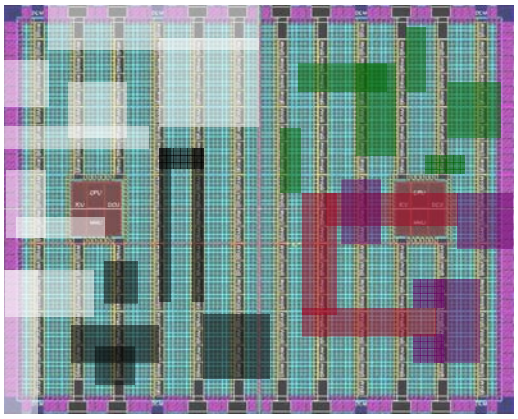
Over 400 Parameterizable Soft Cores

Connectivity

Parallel	Serial
PCI	10 &1 GE MACs
PCI-X	Ethernet PHYs
SPI-4	XAUI
SPI-3	PCI Express
XGMII	Aurora
Many more …	Many more …

General Purpose

CORE Generator
- Building Blocks
- Memory Generators
- IOB Configurations
- Arithmetic and Shifters
- Registers
- Buffers
- Many More …



DSP & Math

Advanced	Math
Reed-Solomon	Multipliers
Turbo Codecs	MAC
Virterbi	Divider
Video	Filters
Wireless	CORDIC
Many More …	Many more …

Processor

Peripherals	Infrastructure
Interrupt Controller	CoreConnect Bus
UARTs	Arbiter
Timer	Bridge
GPIO	Memory controllers
SPI	Soft processors
Many more …	Software IP
	Many more …

Plus...
- AllianceCORE™ IP from partners
- Customization by Xilinx Design Services

Available at the Xilinx IP Center: http://www.xilinx.com/ipcenter

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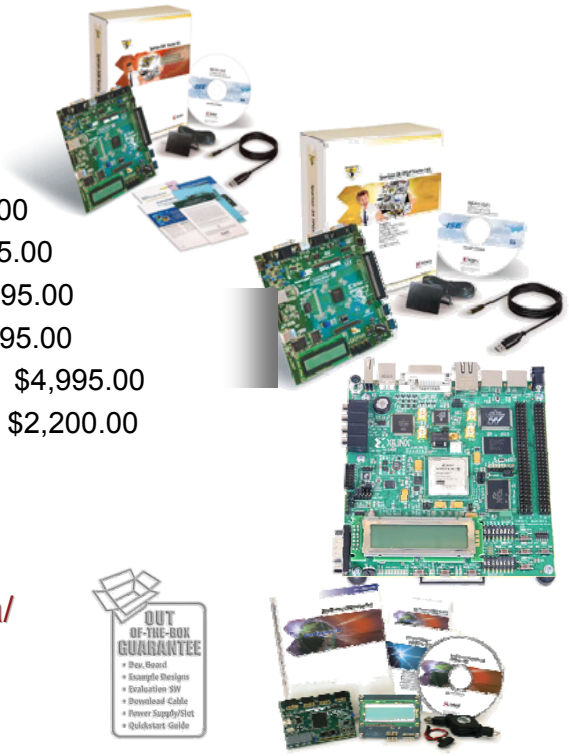
Starter Kits

Evaluate and Get a Jump-Start on Your Design

Spartan-3A Starter Kit — $189.00
Spartan-3AN Starter Kit — $199.00
CoolRunner-II CPLD Starter Kit - $39.00
Virtex-5 LX FPGA ML501 Evaluation Platform — $995.00
Virtex-5 LX FPGA ML505 Evaluation Platform — $1,195.00
Virtex-5 SXT FPGA ML506 Evaluation Platform — $1,195.00
Virtex-5 FXT FGPA ML507 Evaluation Platform — $1,195.00
Virtex-5 LXT FPGA ML521 RocketIO Char. Platform — $4,995.00
Virtex-5 LXT FPGA ML550 Netw. I/F & Pwr Platform — $2,200.00



And many more from Xilinx, distributors and partners

- www.xilinx.com/products/devboards/
- http://www.nuhorizons.com/xilinx/fpga/

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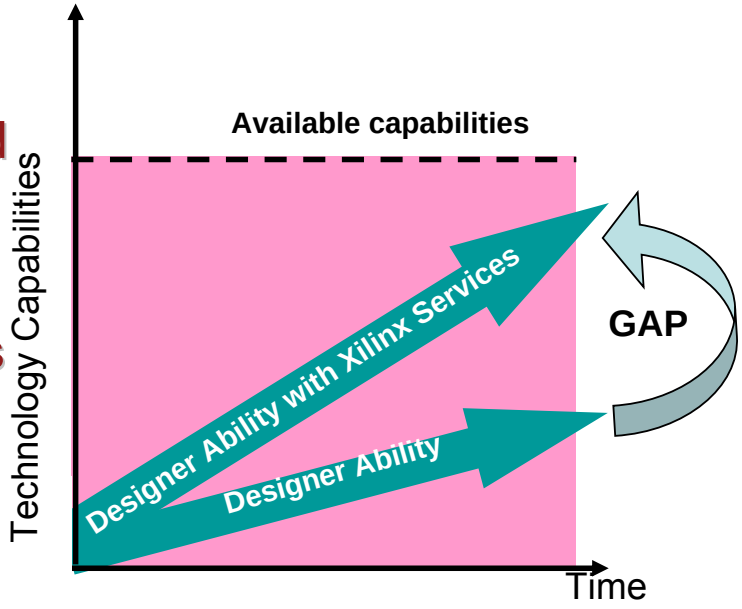
Services

Go to Market Faster - Decrease Design Time and Mitigates Risk

Close the "Technology Gap" with Xilinx Services Portfolio

- Design Services
- Titanium Dedicated Engineering
- QuickStart!
- Education Services



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Nu Horizons Customer Seminars

Entwurf von Digitalen Schaltungen mit FPGAs	Berlin	30.09.2008
Digitale Signalverarbeitung (DSP) mit FPGAs	Frankfurt	01.10.2008
Embedded Prozessoren mit FPGAs	Freiburg	02.10.2008
PCIe	Frankfurt	09.10.2008
PCIe	München	16.10.2008
Entwurf von Digitalen Schaltungen mit FPGAs	München	10.02.2009
Embedded Prozessoren mit FPGAs	Zürich	30.03.2009
Entwurf von Digitalen Schaltungen mit FPGAs	Frankfurt	07.04.2009
Digitale Signalverarbeitung (DSP) mit FPGAs	Frankfurt	08.04.2009
Embedded Prozessoren mit FPGAs	Stuttgart	23.04.2009
Digitale Signalverarbeitung (DSP) mit FPGAs	Stuttgart	21.09.2009
Entwurf von Digitalen Schaltungen mit FPGAs	Stuttgart	22.09.2009
Embedded Prozessoren mit FPGAs	Frankfurt	05.10.2009
Entwurf von Digitalen Schaltungen mit FPGAs	Zürich	12.10.2009
Digitale Signalverarbeitung (DSP) mit FPGAs	Zürich	13.10.2009
Entwurf von Digitalen Schaltungen mit FPGAs	Berlin	27.10.2009
Digitale Signalverarbeitung (DSP) mit FPGAs	München	19.11.2009

http://de.nuhorizons.com/seminars/index.asp

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Agenda

- ***Foundation***
- ***Connectivity Solutions***
- ***Embedded Solutions***
- ***Signal Processing***
- ***Reference: Product Tables***

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Why Xilinx for Connectivity?

- *Adapts to emerging standards*
- *Allows changes to evolving standard specifications*
- *Minimizes time for "re-spins"*
- *Provides future proofing*
- *System tools for integration*

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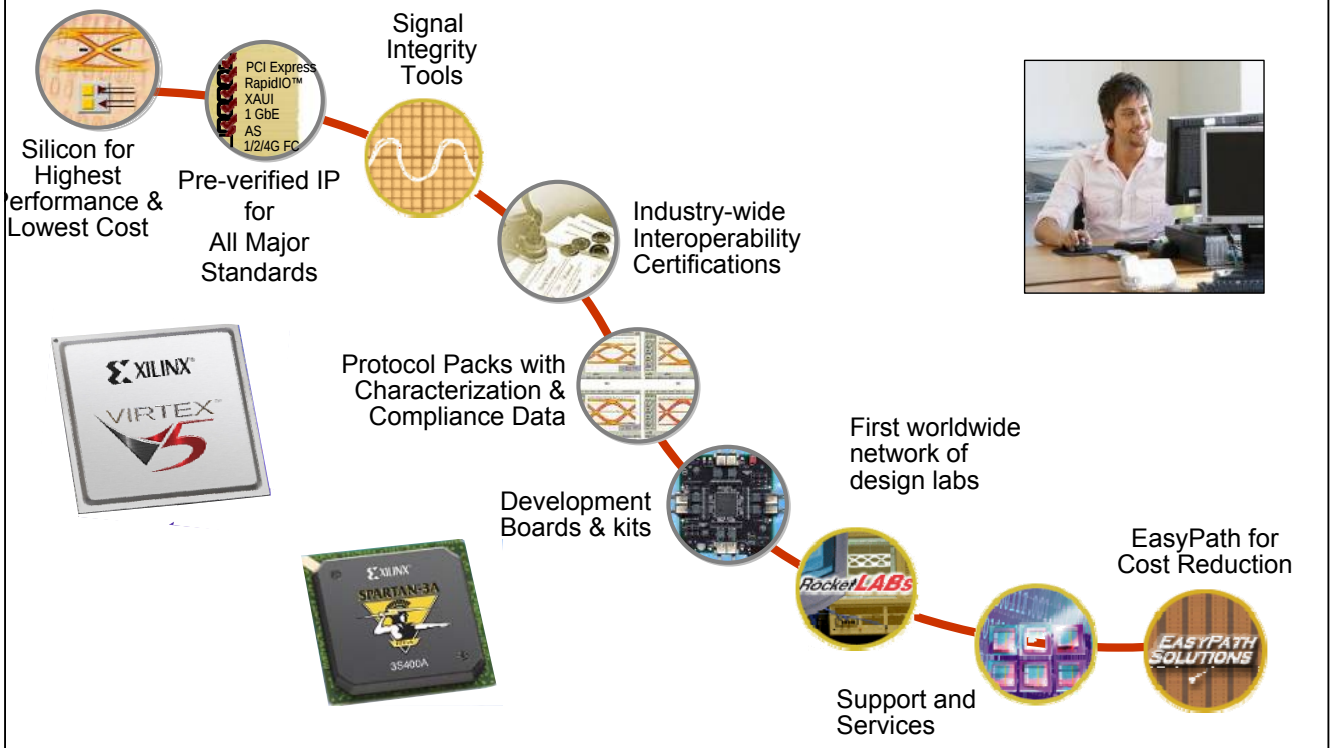
Connectivity Solutions Overview

Flexibility to Adapt to Evolving Standards and Scale for Future Needs



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Xilinx Connectivity IP

PCI & PCI Express

- $ PCI Express x1, x4, & x8 PCI Express Wrapper (Hard Block)
- $ PCI Express PIPE
- $P PCI-X 64/133
- $P PCI 64/66
- $PS PCI 32/33
- C 32/33 XPS Full Bridge

Memory Functions

- P FIFO Generator (Asym. ports/Independent Clk Domains)
- P Memory Generator (Distributed Memory/ Block Memory)
- P CAM (SRL16 & Block Memory)

Wired Networking & Telecom

- $P GFP-Transparent & Frame Mapped
- $P SPI-4.2 (POS-PHY L4)
- $ SPI-4.2 Lite (reduced area,1/4 rate)
- $ SPI-3 (POS-PHY L3) LINK
- $ SPI-3 (POS-PHY L3) PHY
- P Packet Queue Quad SPI-3 to SPI-4.2 Bridge Ref Des.
- $ RapidIO Serial (x1 & 4) PHY Layer
- $ RapidIO Logical Layer

Automotive

- $P CAN
- $P MOST
- $P FlexRay

Ethernet & Storage

- $P 10 Gb Ethernet MAC
- P XAUI XGMII Ref Des.
- $P Tri-Mode Ethernet MAC
- $P 1 Gb Ethernet MAC
- P 1 Gb Ethernet PCS/PMA-SGMII
- P Ethernet Statistics
- $PC 10/100 Mb Ethernet MAC
- $P 1, 2, & 4 Gb FibreChannel

$ - License Fee, P - Parameterized, C- CoreConnect I/F, S - Project License Available

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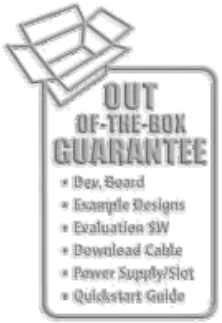
Connectivity Hardware Platforms

Complete Solution in a Box to Help You Get Started Quickly

Connectivity Kits
- Board
- Built-in/evaluation IP
- System examples & Ref designs
- Device drivers, GUI



Virtex-5 PCI Express Kit

Virtex-5 Gb Ethernet Kit

Spartan-3 PCI Express Kit

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Embedded Applications

- ***Ideal mix of peripherals***
  - Difficult to find the required mix of peripherals in Off The Shelf (OTS) microcontrollers
- ***Adapt to changing requirements***
  - Selecting a single discrete processor core with long-term solution viability is difficult at best
- ***Avoid obsolescence***
  - Without direct ownership of the processing solution, obsolescence is always a concern
- ***Reducing cost, board complexity***
  - Many microprocessor based solutions provide limited on-chip peripheral support

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Embedded Solutions Overview

The Most Flexible Configurable Processing Solutions

ChipScope Debug Tools

Embedded Tools

SW & Programming Platform

- *Protocol Stacks*
- *Device Drivers*
- *BSP Generation*
- *Source Included*
- *Virtual Board*

IP Library

3rd Party

Reference Designs

- *MicroBlaze Linux Reference design*
- *Gigabit System Reference Design*
- *APU/FPU*
- *Applications/Reference Design*
- *Multiple Processors*

others...

Integrated Kits

Development Boards

Documentation & Training

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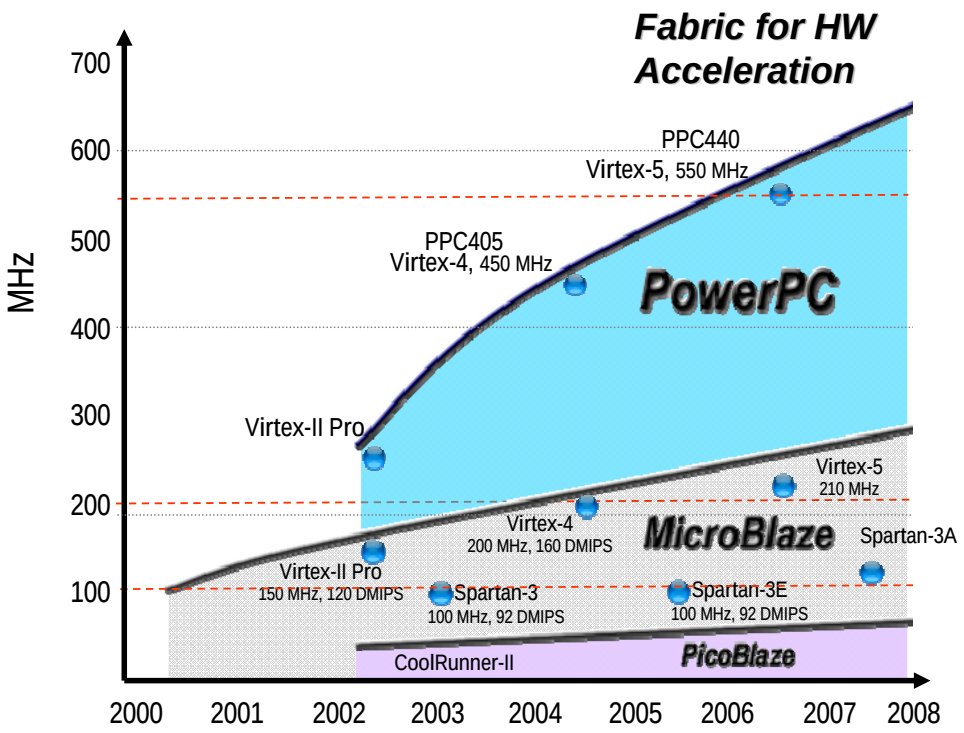
Embedded Processor Portfolio



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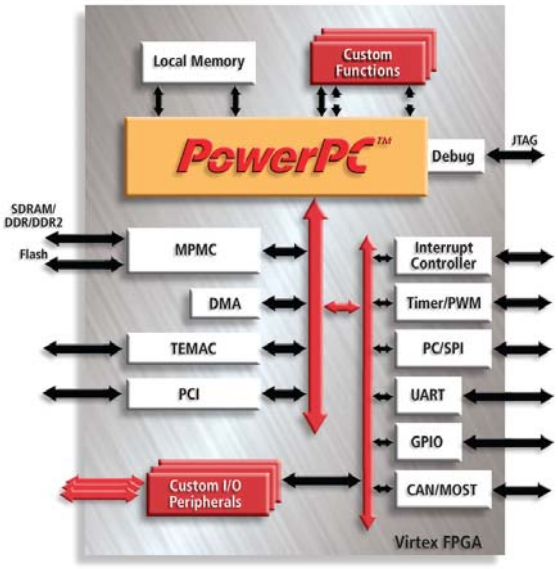
PowerPC - Flexible ASSP Solution

Processor	
Processor (CPU) Type	32-bit
Processor Architecture	PowerPC 440 or 405 RISC processor, MMU
Processor Frequency	25 Mhz to 550 Mhz

Peripherals (IP cores)	
Memory	On-Chip RAM, Flash, SRAM, SDRAM, DDR
Basic IP Peripherals	Timer, Interrupt Controller, UART, GPIO
Advanced Peripherals	Ethernet, CAN, MOST, USB, PCI, TEMAC, FPU, ***Custom***

Software	
RTOS	Linux, VxWorks, QNX, Nucleus, ThreadX, Integrity, LynxOS, eCos, NetBSD
Languages	Assembly, C/C++
Tools	EDK & Platform Studio tool suite, GNU Tools, Eclipse IDE, Wind River Workbench, Green Hills Multi, Mentor Nucleus EDGE, Lauterbach T32, Computex F-Sight, LynuxWorks Luminosity, Agilent FPGA DynamicProbe



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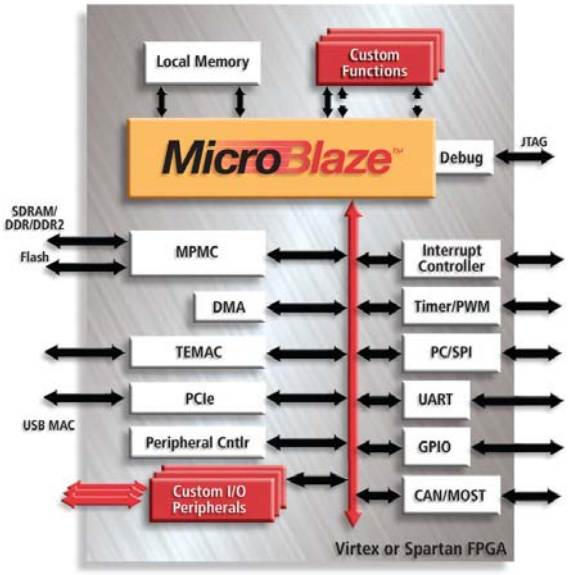
MicroBlaze: Flexible Microcontroller Solution

Processor	
Processor (CPU) Type	32-bit
Processor Architecture	MicroBlaze - RISC processor with MMU
Processor Frequency	25 Mhz to 210 Mhz

Peripherals (IP cores)	
Memory	On-Chip RAM, Flash, SRAM, SDRAM, DDR
Basic IP Peripherals	Timer, Interrupt Controller, UART, GPIO
Advanced IP Peripherals	Ethernet, CAN, MOST, USB, PCI, TEMAC, FPU, ***Custom***

Software	
RTOS	Linux, uClinux, Nucleus, ThreadX, uC/OS-II, uITRON
Languages	Assembly, C/C++
Tools	EDK & Platform Studio tool suite, GNU Tools, Eclipse IDE, Nucleus EDGE, Lauterbach T32, Computex F-Sight, LynuxWorks Luminosity, Agilent FPGA DynamicProbe



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Embedded Development Environment (EDK)

- Define MicroBlaze™ or PowerPC® based systems
  - Implement systems that interface to programmable logic
  - EDK includes MicroBlaze processor core and peripheral IP
- Complete HW and SW development environment
  - Award winning Xilinx Platform Studio
    - Generate custom hardware platform
    - Generate Board Support Packages “on-the-fly”
    - ‘C’ development using GNU Compiler, ‘C’ Libraries
  - Powerful platform debug capabilities
    - Debug hardware using Xilinx ChipScope Pro bus analyzer
    - Debug software with GDB and Xilinx Debug Engine (XMD)
  - Utilize complete reference and application examples to speed development

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Embedded Hardware Platforms

Integrated Development Kits to Kick-Start Your Design

- Standalone Boards:
  - ML5* boards
  - ML4* boards
  - ML3* boards
  - SP3* Starter Kits
  - SP3ADSP
- Development Kits*:
  - PPC & MB ML403
  - V-5 PPC ML507
  - MB SP31600E
  - MB SP3ADSP (coming soon)

* Kits include: HW, SW, Cables, JTAG Probe, & Ref Designs

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NU HORIZONS ELECTRONICS

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- ***Foundation***
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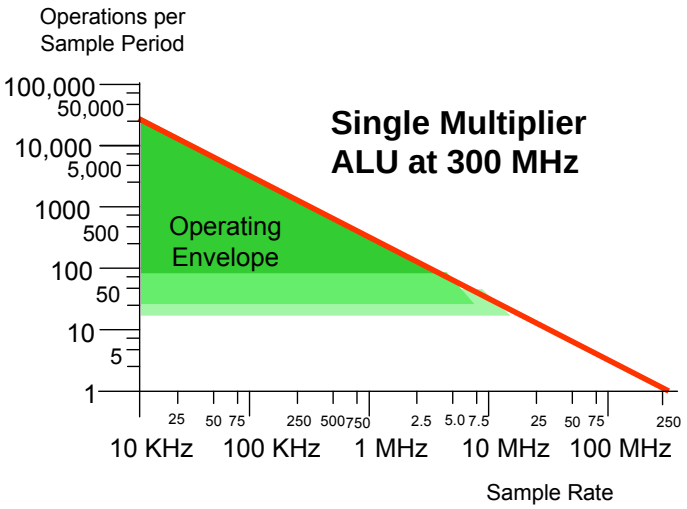
Limits of a DSP Processor

Sample Rate	Operations per sample period	
	Single Multiplier ALU at 300 MHz	Two Multipliers ALU at 600 MHz
8 KHz	37,500	150,000
44.1 KHz	6,803	27,210
300 KHz	1,000	4,000
1.2288 MHz	244	976
3.84 MHz	78	312
27 MHz	11	44
74 MHz	4	16
102.4 MHz	3	12
300 MHz	1	4



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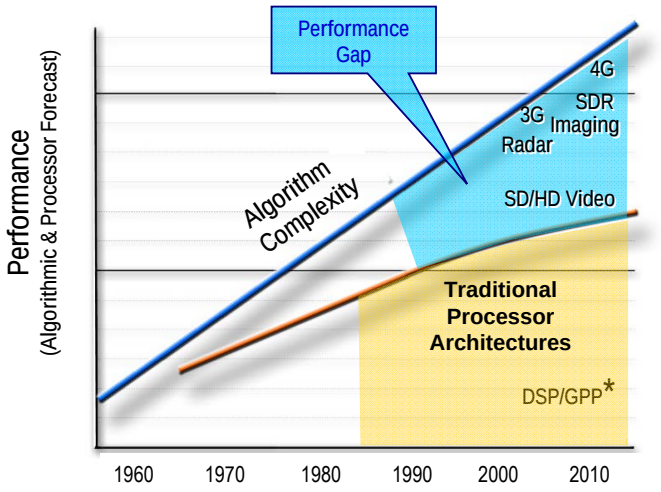
FPGA's Address DSP Performance Gap



* Source: Jan Rabaey, BWRC (Berkeley Wireless Research Center)

Parallelism	→	Performance increase
Flexible architecture	→	Low risk
Easy changes/design migration	→	Handle changing/adding standards
Programmability	→	Customized & differentiated solutions
Technology shrinks	→	Price decreases
Lower power consumption	→	Portable applications

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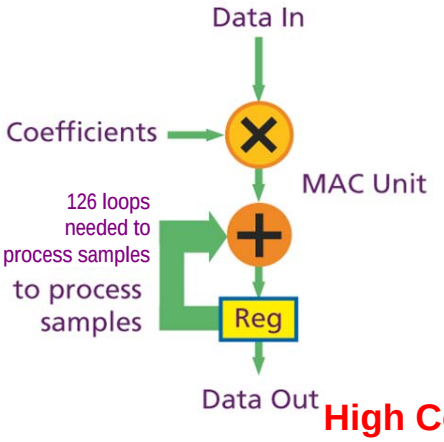
Why FPGAs for DSP?

Conventional DSP Processor - Serial

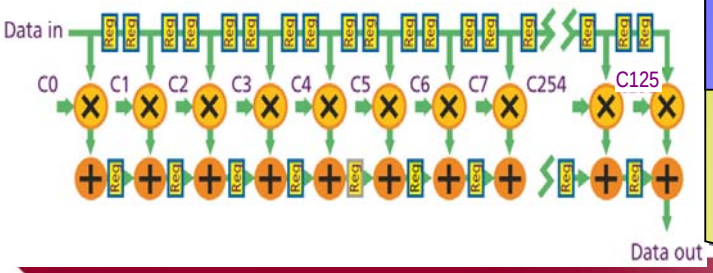


1 GHz / 126 clock cycles = 8 MSPS / MAC unit

MSPS = Megasamples per second

High Computational Workloads

FPGA-based DSP - Parallelism



Virtex FPGA: 550 MHz / 1 clock cycle = 550 MSPS x5 filters

Spartan FPGA: 250 MHz / 1 clock cycle = 250 MSPS

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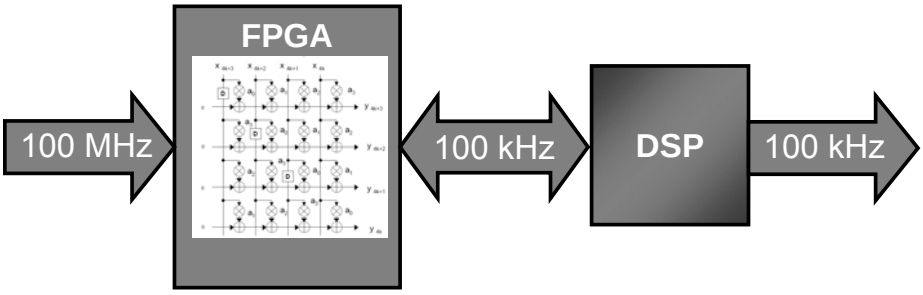
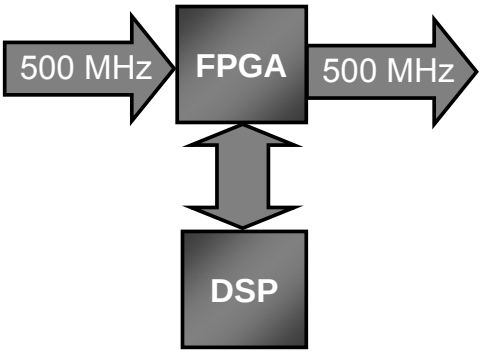
How To Address the DSP Performance Gap?

Pre-processor



Co-processor



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DSP Solutions Overview

Market & Applications Optimized Solutions

Wireless | SDR | Co-processing Kit | Video Developer Kit | Starter Kit

XtremeDSP

XtremeDSP Solution Building Blocks

Platform Studio	Sysgen	AccelDSP	*Development Environments*
ISE			
FFT, FIR Compiler, DUC, DDC, CFR			*DSP Libraries*
Spartan3A-DSP Starter Board	ML506 Virtex-5 SXT Development Board		*Boards*
Spartan-3A DSP	Virtex-5 SXT		*Silicon*

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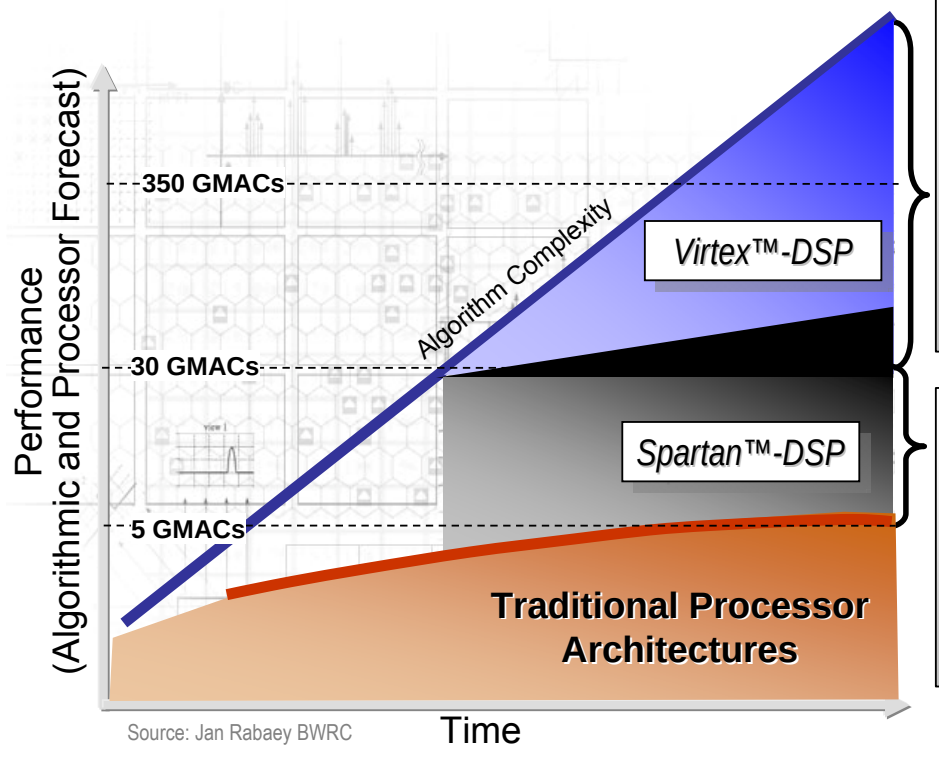
DSP Solution Portfolio



- 3D Medical Imaging
- Wireless Base Stations
- HD Audio/Video Broadcast
- Radar & Sonar
- HD Video Surveillance
- Mobile Software Defined Radio
- MIMO

- Ultrasound
- Pico/Femto Base Stations
- Consumer Video
- SD/HD Video Surveillance
- Mobile Software Defined Radio

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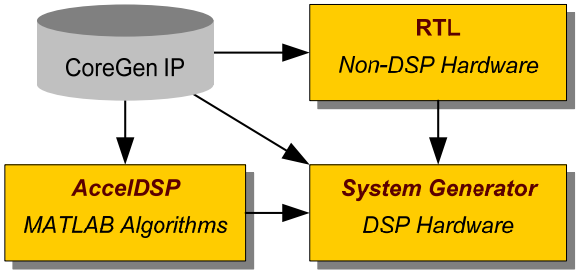
Xilinx DSP IP



- **Over 90 DSP building blocks pre-optimized for Xilinx devices**
  - **Developed by Xilinx DSP hardware design experts**
- **Integrated IP design flow into logical and DSP design environment**

Category	Blocks
Math	mult, adder, accumulator, divider, trig
Filters	FIR, CIC, DAFIR
Memory	RAM, register, FIFO, shift register
Transforms	FFT, IFFT
Processors	MicroBlaze, VLYNQ, SRIO
Video	scalar, 2D FIR, color-space converter, chroma resampler, 2D rank order filter, VOIP
Communications	DDS, CIC, Viterbi Dec, Reed-Solomon Enc/Dec, DDC / DUC, interleaver / deinterleaver

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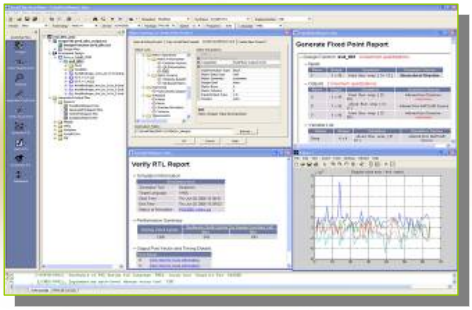
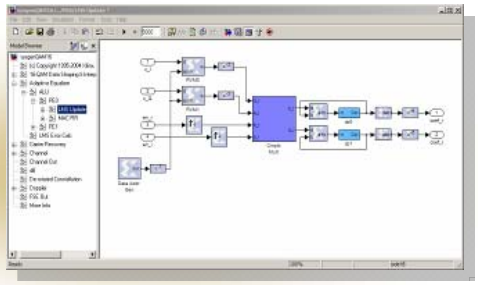
DSP Development Environment

- Comprehensive DSP model-based design flow from The Mathworks MATLAB® and Simulink® environments
  - AccelDSP Synthesis
    - MATLAB to FPGAs
    - Algorithmic exploration
  - System Generator for DSP
    - Simulink to FPGAs
    - Simulink algorithm acceleration
  - Mixed flows
    - RTL / System Generator / AccelDSP / 3rd Party tools

AccelDSP MATLAB to gates



System Generator Simulink to Gates



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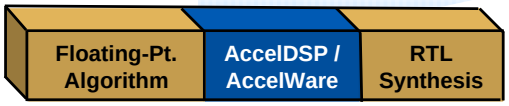
AccelDSP + AccelWare Design Flow

Typical MATLAB DSP Design Flow

Steps performed by AccelDSP



AccelDSP Design Flow

"We saw a 30% reduction in the design cycle time. This equated to an overall project development reduction of 15 percent, which provides two very significant benefits: we get our products to market faster and our teams are freed up to work on other projects sooner."

Dr. Paul Turner
Principal Systems Engineer
Powerwave Technologies

- ***Replaces manual steps***
  - Floating to fixed-point conversion
  - RTL creation
  - RTL and gate verification back to the original algorithm
  - IP creation and integration

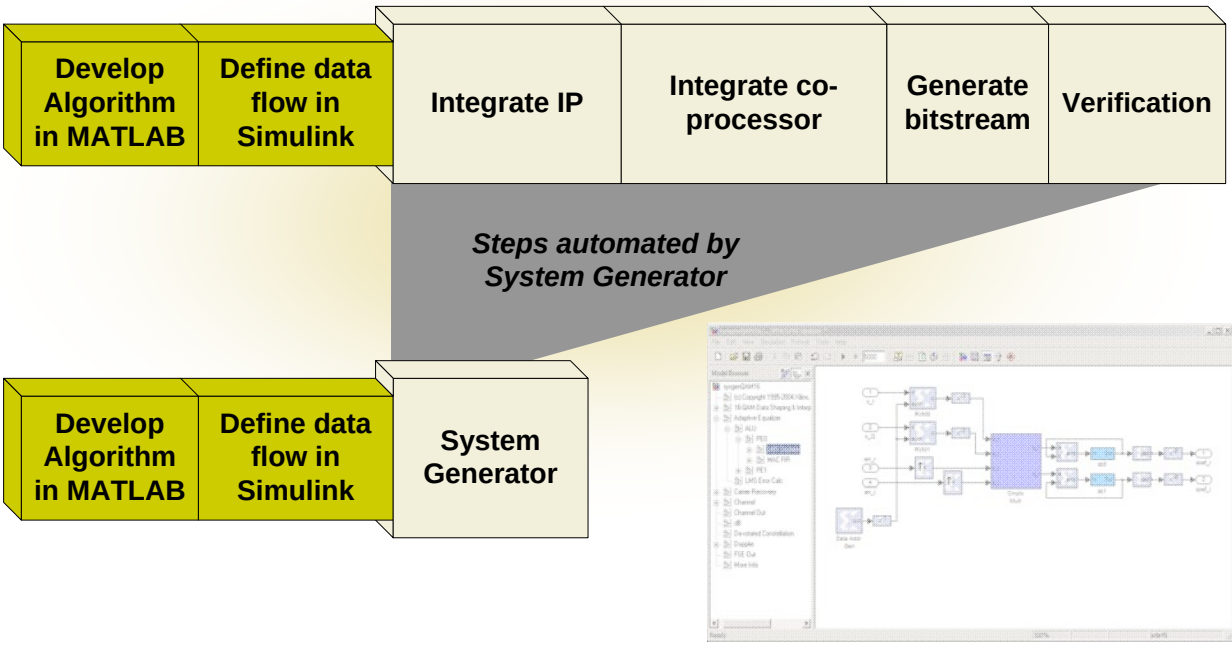
AccelWare DSP IP Core Generators

AccelWare Advanced Math Toolkit	AccelWare Signal Processing Toolkit	AccelWare Communications Toolkit
Polynomial Evaluator	CIC Decimator / Interpolator	A/D Sinc Compensation Filter
QRD-RLS Spatial Filter	Decimating FIR filter	Convolutional Interleaver / Deinterleaver
Givens Array Rotation	FFT, IFFT	Convolutional Encoder
Matrix inversion	FIR Filter	Direct Digital Synthesizer
QR method	Half-Band FIR Filter	Reed-Solomon Decoder
Cholesky	Polynomial Evaluation	Reed-Solomon Encoder
Triangular	Polyphase FIR Filter	BCH Encoder / Decoder
Matrix factorization		Root-raised Cosine Filter
QR method		Viterbi Decoder
Cholesky		Scrambler / Descrambler
SVD		
Triangular System of Equations Solver		

Each Toolkit core provides multiple silicon architectures that are fully parameterized to meet market-specific needs

System Generator Design Flow

Typical graphical based design flow



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DSP Hardware Platforms

Accelerates DSP Development on Xilinx FPGAs

- Include all required hardware, software and cables
- Utilizes reference designs and examples

XtremeDSP Starter Kit – Spartan-3A DSP Edition
XtremeDSP Development Kit – Virtex-5 DSP Edition
XtremeDSP Video Development Kit – Spartan-3A DSP Edition

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Agenda

- *Foundation*
- *Connectivity Solutions*
- *Embedded Solutions*
- *Signal Processing*
- *Reference: Product Tables*

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Virtex-5 LX Platform

	5VLX30	5VLX50	5VLX85	5VLX110	5VLX155	5VLX220	5VLX330
Logic Cells	30,720	46,080	82,944	110,592	155,648	221,184	331,776
LUT6/Flip-Flops	19,200	28,800	51,840	69,120	97,280	138,240	207,360
Distributed RAM (Kbits)	320	480	840	1,120	1,640	2,280	3,420
Total Block RAM (Kbits)	1,152	1,728	3,456	4,608	6,912	6,912	10,368
Clock Management Tiles	2	6	6	6	6	6	6
DSP48E Slices	32	48	48	64	128	128	192
EasyPath	No	No	Yes	Yes	Yes	Yes	Yes
Package	**Size (mm)**						
FF324	19	220	220					
FF676	27	400	440	440	440			
FF1153	35		560	560	800	800		
FF1760	42.5				800	800	800	1,200

X = Number of SelectIO

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Virtex-5 LXT Platform

	5VLX20T	5VLX30T	5VLX50T	5VLX85T	5VLX110T	5VLX155T	5VLX220T	5VLX330T
Logic Cells	19,968	30,720	46,080	82,944	110,592	155,648	221,184	331,776
LUT6/Flip-Flops	12,480	19,200	28,800	51,840	69,120	97,280	138,240	207,360
Total Distributed RAM (Kbits)	210	320	480	840	1,120	1,640	2,280	3,420
Total Block RAM (Kbits)	936	1,296	2,160	3,888	5,328	7,632	7,632	11,664
Clock Management Tiles	1	2	6	6	6	6	6	6
DSP48E Slices	24	32	48	48	64	128	128	192
RocketIO GTP Channels	4	8	12	12	16	16	16	24
PCIe Endpoint Blocks	1	1	1	1	1	1	1	1
10/100/1000 EMACs	2	4	4	4	4	4	4	4
EasyPath	No	No	No	Yes	Yes	Yes	Yes	Yes
Package / **Size (mm)**								
FF323 / 19	172,4	172,4						
FF665 / 27		360,8	360,8					
FF1136 / 35			480,12	480,12	640,16	640,16		
FF1738 / 42.5					680,16	680,16	680,16	960,24

X,Y — X = SelectIO, Y=RocketIO Channels

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Virtex-5 SXT Platform

	5VSX35T	5VSX50T	5VSX95T	5VSX240T
Logic Cells	34,816	52,224	94,208	239,616
LUT6/Flip-Flops	21,760	32,640	58,880	149,760
Total Distributed RAM (Kbits)	520	780	1,520	4,200
Total Block RAM (Kbits)	3,024	4,752	8,784	18,576
Clock Management Tiles (CMT)	2	6	6	6
DSP48E Slices	192	288	640	1,056
RocketIO GTP Channels	8	12	16	24
PCIe Endpoint Blocks	1	1	1	1
10/100/1000 EMACs	4	4	4	4
EasyPath	No	Yes	Yes	Yes
Package / **Size (mm)**				
FF665 / 27	360,8	360,8		
FF1136 / 35		480,12	640,16	
FF1738 / 42.5				960,24

X,Y — X = SelectIO, Y=RocketIO Channels

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Virtex-5 FXT Platform

	5VFX30T	5VFX70T	5VFX100T	5VFX130T	5VFX200T
Logic Cells	32,768	71,680	102,400	131,072	196,608
LUT6/Flip-Flops	20,480	44,800	64,000	81,920	122,880
Total Distributed RAM (Kbits)	380	820	1,240	1,580	2,280
Total Block RAM (Kbits)	2,448	5,328	8,208	10,728	16,416
Clock Management Tiles	2	6	6	6	6
DSP48E Slices	64	128	256	320	384
RocketIO GTX Channels	8	16	16	20	24
PowerPC 440 Processors	1	1	2	2	2
PCIe Endpoint Blocks	1	3	3	3	4
10/100/1000 EMACs	4	4	4	6	8
EasyPath	No	Yes	Yes	Yes	Yes
Package / **Size (mm)**					
FF665 / 27	360,8	360,8			
FF1136 / 35		640,16	640,16		
FF1738 / 42.5			680,16	840,20	960,24

X,Y X = SelectIO, Y=RocketIO Channels

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Cross-Platform Compatibility

		LXT Platform								SXT Platform				FXT Platform				
		20T	30T	50T	85T	110T	155T	220T	330T	35T	50T	95T	240T	30T	70T	100T	130T	200T
Logic Cells		20K	30K	50K	85K	110K	155K	220K	330K	35K	50K	95K	240K	30K	70K	100K	130K	200K
Block RAM (Mbits)		0.9	1.3	2.2	3.9	5.3	7.6	7.6	11.6	3.0	4.8	8.8	18.6	2.4	5.3	8.2	10.7	16.4
DSP48E Slices		24	32	48	48	64	128	128	192	192	288	640	1,056	64	128	256	320	384
RocketIO GTP Channels		4	8	12	12	16	16	16	24	8	12	16	24					
RocketIO GTX Channels														8	16	16	20	24
PowerPC 440 Processors														1	1	2	2	2
PCIe Endpoint Blocks		1	1	1	1	1	1	1	1	1	1	1	1	1	3	3	3	4
10/100/1000 EMACs		2	4	4	4	4	4	4	4	4	4	4	4	4	4	4	6	8
Package	Size (mm)																	
FF323	19	172,4	172,4															
FF665	27		360,8	360,8						360,8	360,8			360,8	360,8			
FF1136	35			480,12	480,12	640,16	640,16				480,12	640,16			640,16	640,16		
FF1738	42.5					680,16	680,16	680,16	960,24				960,24			680,16	840,20	960,24

X,Y X = SelectIO, Y=RocketIO Channels

Change device with no board redesign to change logic/BRAM/DSP quantity

*"T" Platforms are Pin Compatible in the Same Package**

* Note: must have adjustable regulator on AVCCPLL for GTP to GTX migration

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Extended Spartan-3A Family

Extended Spartan-3A Resources by Device		Devices						
		3S50A	3S200A	3S400A	3S700A	3S1400A	3SD1800A	3SD3400A
System Gates		50K	200K	400K	700K	1400K	1800K	3400K
Logic Cells		2K	4K	8K	13K	25K	37K	54K
Distributed RAM (max)		11K	28K	56K	92K	176K	260K	373K
18k BRAM Blocks		3	16	20	20	32	84	126
BRAM Kbits		54	288	360	360	576	1512	2268
Digital Clock Managers		2	4	4	8	8	8	8
Multipliers / DSP48A Blocks		3 / 0	16 / 0	20 / 0	20 / 0	32 / 0	0 / 84	0 / 126
Integrated Device DNA Security		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Single Chip Nonvolatile Option		Yes	Yes	Yes	Yes	Yes	No	No
	Size (Pitch) in mm							
VQ100	16x16 (0.5)	68	68					
TQ144	22x22 (0.5)	108*						
FT256	17x17 (1.0)	144	195*	195	161	161		
FG320	19x19 (0.8)		248	251				
FG400	21x21 (1.0)			311*	311			
FG484	23x23 (1.0)				372*	375		
CS484	19x19 (1.0)						309	309
FG676	27x27 (1.0)					502*	519	469

New!!

* Single Chip Non-Volatile Option Available for this package

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CoolRunner-II Family Overview

Features	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
F_{SYSTEM} (MHz)	323	263	244	256	217	179
Max User I/O	33	64	100	184	240	270
I/O Banks	2	2	2	2	4	4
LVCMOS, LVTTL (1.5,1.8,2.5,3.3)	Yes	Yes	Yes	Yes	Yes	Yes
HSTL, SSTL	-	-	Yes	Yes	Yes	Yes
DualEDGE	Yes	Yes	Yes	Yes	Yes	Yes
DataGATE, CoolCLOCK	-	-	Yes	Yes	Yes	Yes
Standby Power (µW)	28.8	30.6	34.2	37.8	41.4	45.0
Standby Power (µA)	16.0	17.0	19.0	21.0	23.0	25.0
Advanced Security	Yes	Yes	Yes	Yes	Yes	Yes

Packages (size)	Maxium User I/O					
QFG32 (5x5 mm)	21					
VQ44 (12x12 mm)	33	33				
QF48 (7x7 mm)		37				
CP56 (6x6 mm)	33	45				
VQ100 (16x16 mm)		64	80	80		
CP132 (8x8 mm)			100	106		
TQ144 (22x22 mm)			100	118	118	
PQ208 (30.6x30.6 mm)				173	173	173
FT256 (17x17 mm)				184	212	212
FG324 (23x23 mm)					240	270

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ISE Design Suite Overview

ISE Foundation (EF-ISE-FND)	$2495
• Complete front-to-back logic design flow optimal performance, maximum productivity, and reduced power	
ISE WebPACK	Free and Downloadable
• Free, downloadable design support for all Xilinx CPLDs, and medium-density Xilinx FPGAs	
PlanAhead Design and Analysis Tool (EV-PLNHD)	$2495
• Streamlines the step between synthesis and place-and-route with a design solution to identify and fix problems early	
ChipScope Pro (EF-CSP-PRO)	$695
• Delivers a design solution to verify and debug FPGAs designs on-chip in real time at or near operating system speed	
ChipScope Pro Serial I/O Toolkit (EF-CSP-SIOTK)	$295
• Shorter debug and setup for serial I/O designs costing less than 1% of comparable BERT hardware test equipment	
Platform Studio and the Embedded Development Kit (EDK) – (EF-EDK)	$495
• A pre-configured kit combining award winning design tools as well as all the documentation and IP for designing Xilinx Platform FPGAs with embedded PowerPC® hard processor cores and/or MicroBlaze™ soft processor cores.	
System Generator for DSP (EF-SYSGEN-4SL-PC)	$995
• An environment for FPGA-based DSP systems through creation, simulation, implementation and debug using Simulink from Mathworks, Inc.	
AccelDSP Synthesis Tool (EF-ACDSP-F-PC)	$595
• A high-level MATLAB® language based tool for designing DSP blocks for Xilinx FPGAs	

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ISE Design Suite – Device Support

		ISE *WebPACK*	ISE *Foundation*
Platforms		Microsoft® Windows® XP Professional (32 bit) Microsoft Windows Vista Business (32 bit) Red Hat Enterprise Linux WS 4/5 (32 bit) SUSE Linux Enterprise 10 (32 bit)	Microsoft Windows XP Professional (32 & 64 bit) Microsoft Windows Vista Business (32 & 64 bit) Red Hat Enterprise Linux WS 3/4/5 (32 & 64 bit) SUSE Linux Enterprise 10 (32 & 64 bit)
Devices (FPGA)	Virtex™ Series	Virtex: XCV50 - XCV600 Virtex-E: XCV50E - XCV600E Virtex-II: XC2V40 - XC2V500 Virtex-II Pro: XC2VP2 - XC2VP7 Virtex-4: LX: XC4VLX15, XC4VLX25 SX: XC4VSX25 FX: XC4VFX12 Virtex-5: LX: XC5VLX30, XC5VLX50 LXT: XC5VLX30T, XC5VLX50T FXT: XC5VFX50T Virtex Q: XQV100- XQV600 Virtex QR: XQVR300, XQVR600 Virtex-E Q: XQV600E	Virtex: All Virtex-E: All Virtex-II/Pro: All Virtex-4: LX: All SX: All FX: All Virtex-5: LX: All LXT: All FXT: All Virtex Q/QR: All Virtex-E Q: All
	Spartan™ Series	Spartan-II/IIE: All Spartan-3: XC3S50 - XC3S1500 Spartan-3A: All Spartan-3AN: All Spartan-3A DSP: XC3SD1800A Spartan-3E: All XA (Xilinx Automotive) Spartan-3: All	Spartan-II/IIE: All Spartan-3: All Spartan-3A: All Spartan-3AN: All Spartan-3A DSP: All Spartan-3E: All XA (Xilinx Automotive) Spartan-3: All
Devices (CPLD)	CoolRunner™ XPLA3 CoolRunner-II ™ CoolRunner-IIA XC9500™ Series	All	

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XDS Product Summary

About XDS

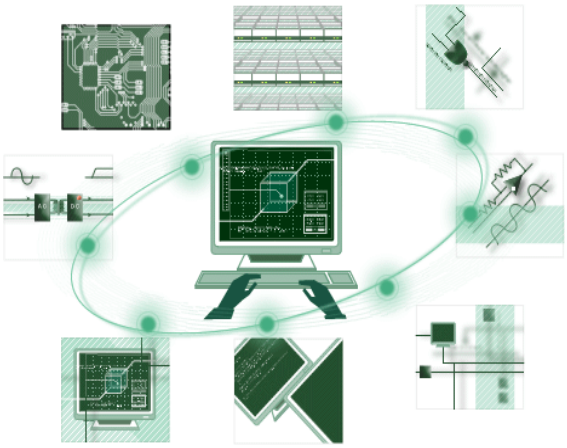
Xilinx Design Services is dedicated to developing FPGA applications for Xilinx customers by employing a flexible design engagement model to cover the entire product development cycle from specification through coding, verification, timing closure and system integration.

XDS Expertise (Embedded processor, Hardware/Software co-design, High-performance logic designs)

Specialists in FPGA Application Design
Veteran Product Development Skills
Diverse Product Design Experience

Benefits of XDS

Project Design & Management
Focused on design quality
Faster time to market for customers
High Performance
Lower Product Cost



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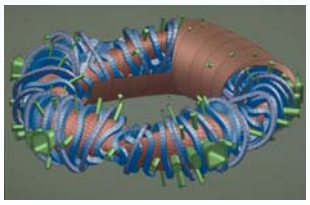
Forschungszentrum Karlsruhe
in der Helmholtz - Gemeinschaft
Institut für Prozessdatenverarbeitung und Elektronik

Die neue Quenchdetection für W7-X

SEI-Tagung 22. - 24.09.2008 / IPP Greifswald

Klaus Petry



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Institut für Prozessdatenverarbeitung und Elektronik

Fahrplan ....

Hardware

(HV-)Technik des Quench-Detektors / Neuheiten / Sicherheitseinrichtungen
Kommunikationsstruktur des QD-Systems / Schaltschrankaufbau

Software / Rechnersysteme

FPGA-Detektor-Firmware

November 2007: PC, RT-System

QVision zur Kalibration, Datensatzverwaltung, Parametrierung
LabView®-Oberfläche zur Bed. des RT-Systems (Q-Ereignisverfolgung)
RT-Systemsoftware (ADWin-Basic)

Heute, Juli 2008: Embedded PC

QVision und Embedded PC ersetzen RT-System
Neu (Add-ON): *Kontrollbetrieb zur Zustands- / Ereignisprotokollierung*

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Live-Demonstration

➔ **QVision-Software**

Parametrierung / Visualisierung (Beispiel: Detektor-Balancierung)
Diagnoseeinrichtungen / Datensatzverwaltung / Hintergrundbetrieb

➔ **Kontrollbetrieb**

Fehlerzustands- und Bedienungs-Ereignisverfolgung
Automatische Datensicherung QRAM-Verlaufsspeicher
Quenchereignisverfolgung / Berechnung der Q-Ereigniszeiten
Quenchereignisprotokollierung / Kontrollbetriebsprotokollierung

Ausblick

Anknüpfungspunkte für weitere Zusammenarbeit mit dem IPP / W7-X
Fertigung von weiteren 420 - 600 Detektoren + Racks + Schaltschränke
Erweiterung der Remoteschnittstelle (WinCC®-Anbindung der Gruppenrechner)
***EU:** Einsatz des IPE-QD-Systems bei ITER ?*

.... Fahrplan

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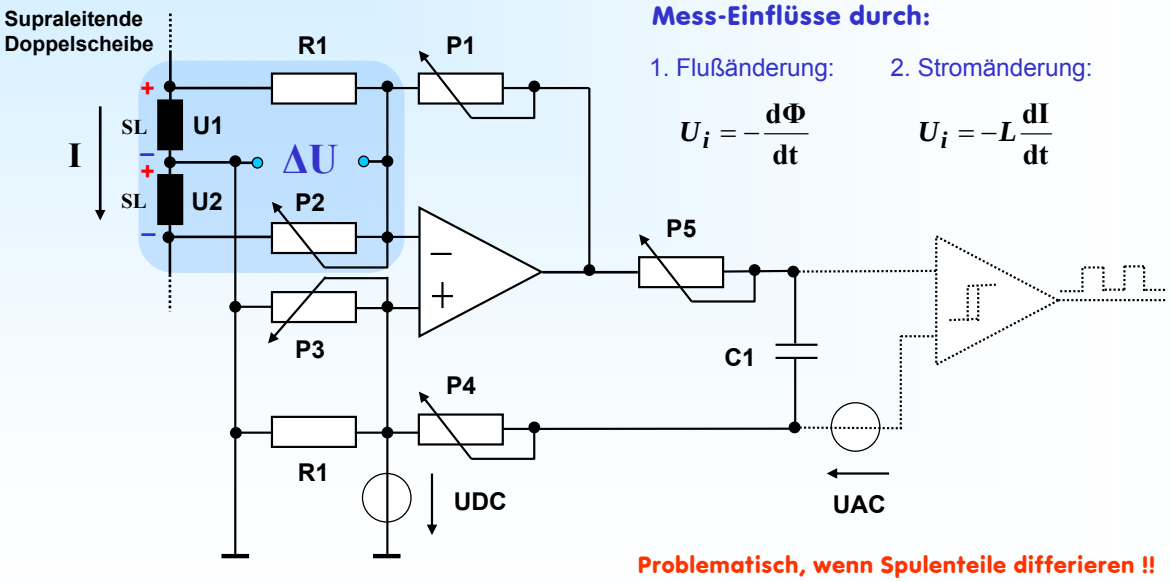
Prinzip der elektronischen Quenchdetection nach Nöther et al. (Spannungsdifferenzpr.)



Mess-Einflüsse durch:

1. Flußänderung: $U_i = -\frac{d\Phi}{dt}$

2. Stromänderung: $U_i = -L\frac{dI}{dt}$

Problematisch, wenn Spulenteile differieren !!

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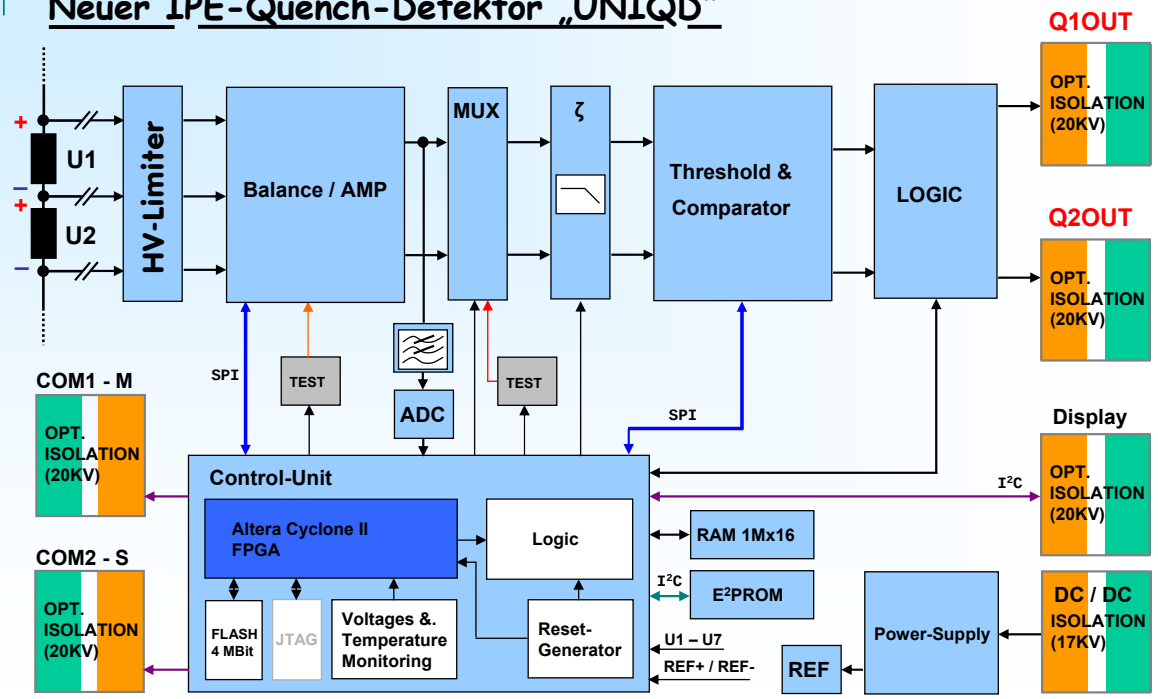
Neuer IPE-Quench-Detektor „UNIQD"



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Quench-Detektoreinschub

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Kommunikationsprotokoll IPE-UNIQD-System:

➔ Kommunikation über „Key-Words“

➔ Offener „Quasi-Industriestandard“

Kommando-Beispiele .....

- **Balance UPOS zu UNEG**

  <2>XXXBALANC(NN)????<3> — Bereich NN: 0 – 255
  Siehe Beschreibung Register R15

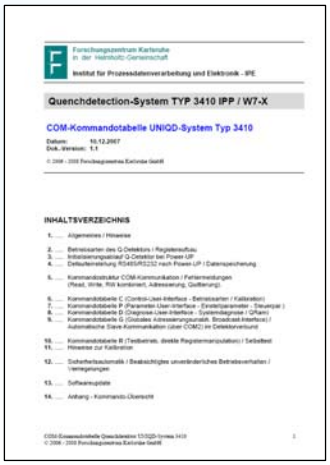
  Antwort:
  <2>XXXQ????<3> — Default: NN = 127
  Bezug: *R15*

- **Positive Komparatorschwelle QD1**

  <2>XXXQ1SPOS(NN)????<3> — Bereich NN: 0 – 255
  Siehe Beschreibung Register R19

  Antwort:
  <2>XXXQ????<3> — Default: NN = 127
  Bezug: *R19*

Register- und Kommandotabelle QD-System (52 Kommandos)


Quenchdetection-System TYP 3410 IPP / W7-X

COM-Kommandotabelle UNIQD-System Typ 3410

INHALTSVERZEICHNIS

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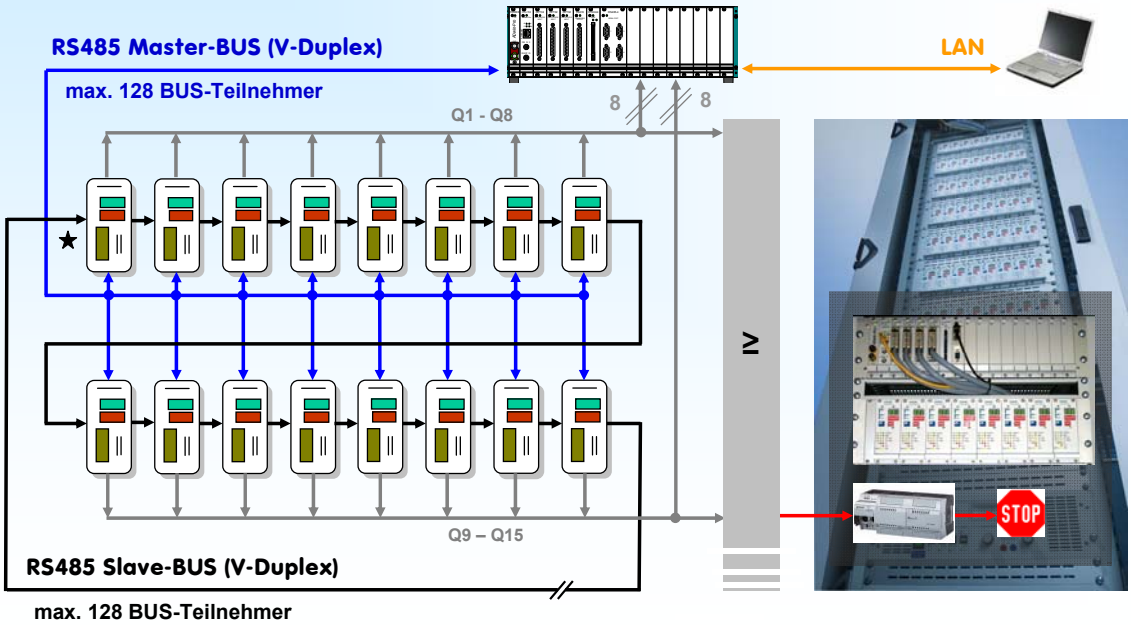
Dual-Bus Kommunikation QD-System / Variante mit RT-System



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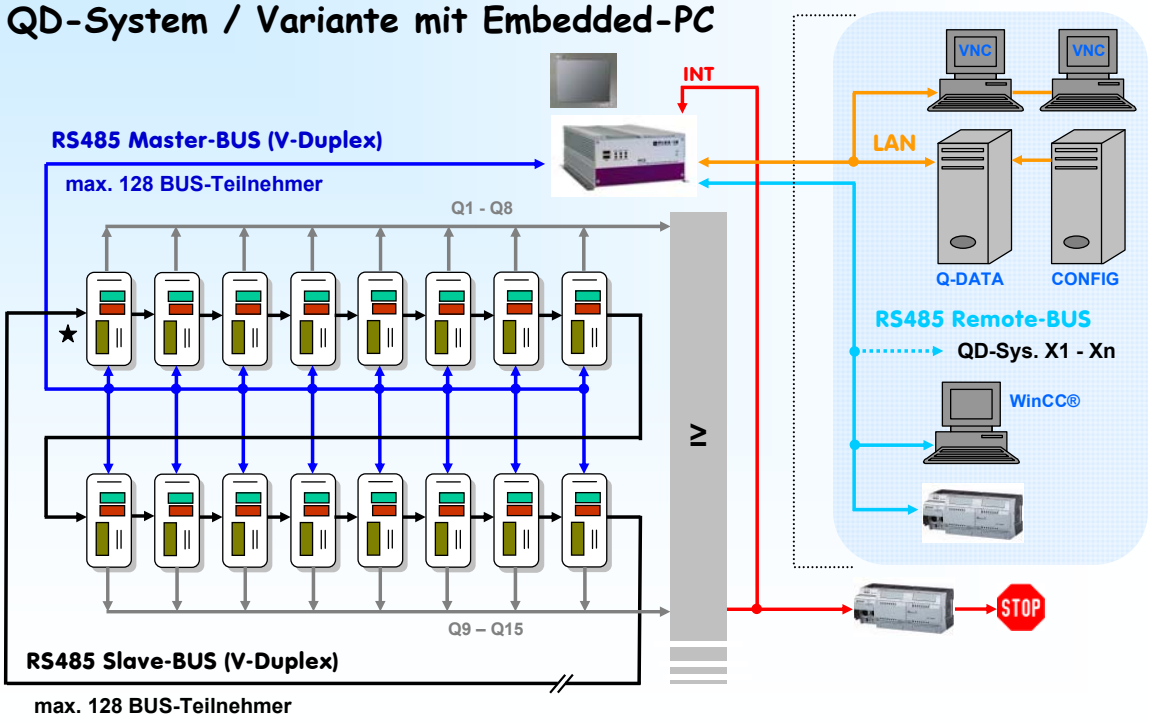
QD-System / Variante mit Embedded-PC



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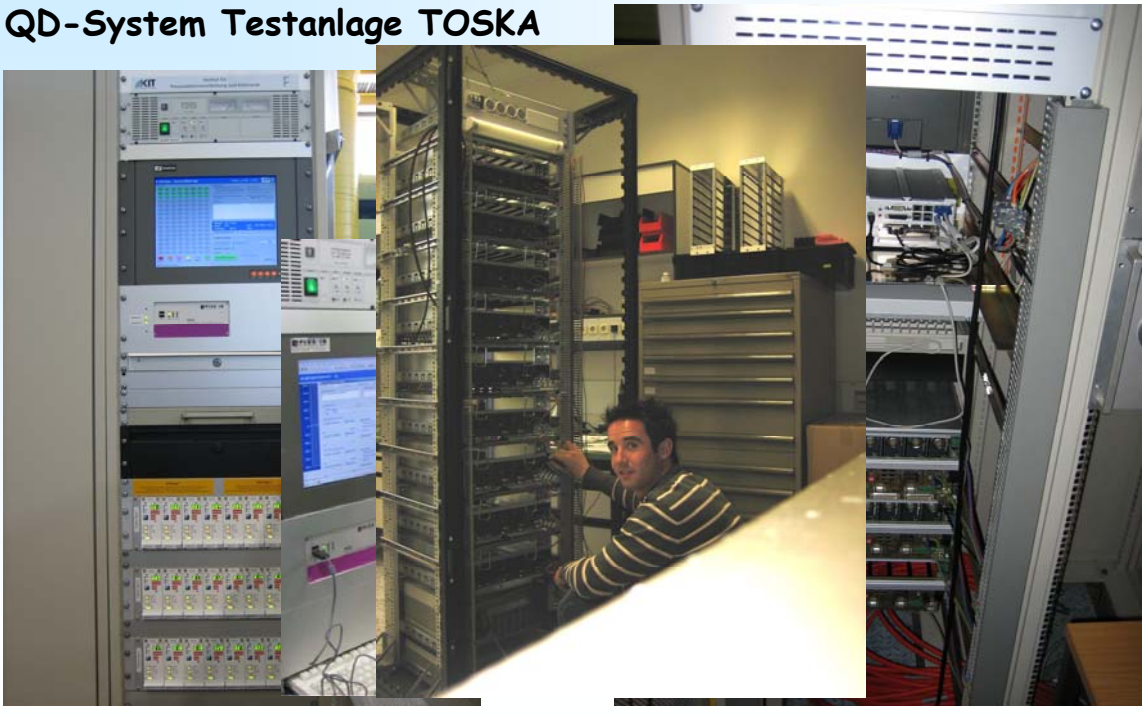
QD-System Testanlage TOSKA



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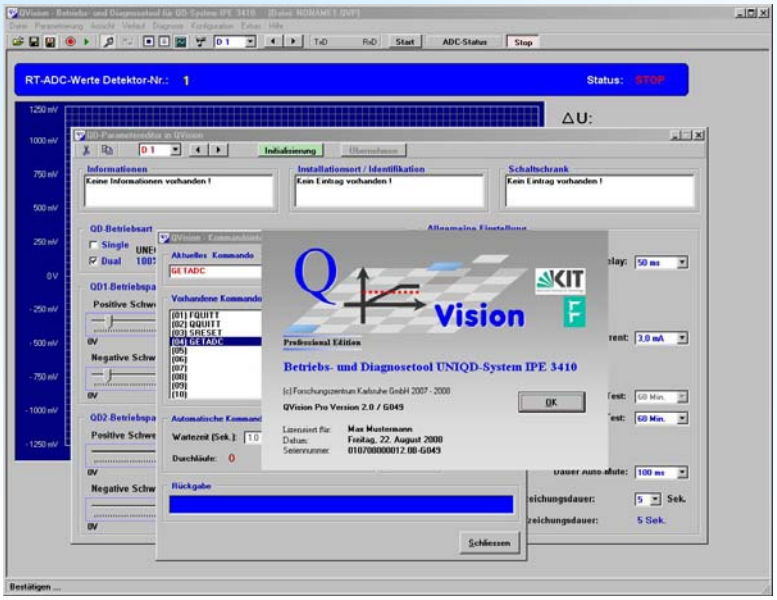
Betriebs- und Diagnosetool „QVision"



Vorführung

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Qualitätsanfordeungen bei der Entwicklung des QD-Systems (IPE)

Temperaturwechsel-Test des QD-Systems

Vibrationstest („Rütteltest")

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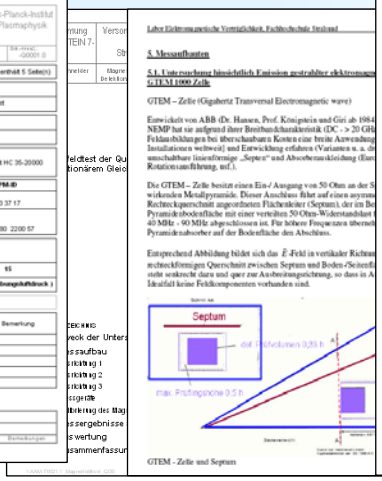
Prüfungen des IPP / Greifswald:

- **HV-Test (20KV gegen PE; 500V / 1000V Eing.)**
- **Magnetfeld (30mT)**
- **EMV-Test / DIN 55022 / EN61000 ff.**



GTEM - Zelle und Septum

FACHHOCHSCHULE STRALSUND
FB ETI, Labor für Elektromagnetische Verträglichkeit
Zur Schwedenschanze 15, 18435 Stralsund

EMV Prüfbericht

Inhalt

1. Allgemeine Angaben zum Prüfgegenstand (Prüfling)
2. Auftraggeber
3. Prüftermine
4. Prüfbedingungen
5. Messaufbauten
   - 5.1. Untersuchung hinsichtlich Emission gestrahlter elektromagnetischer Felder in der GTEM 1000 Zelle (EN 55022)
   - 5.2. Untersuchung hinsichtlich Emission geleiteter Störungen (EN 55022)
   - 5.3. Prüfung der Störfestigkeit gegen die Entladung statischer Elektrizität (ESD) (EN 61000-4-2)
   - 5.4. Prüfung der Störfestigkeit gegen hochfrequente elektromagnetische Felder in der GTEM 1000 Zelle (EN 61000-4-3)
   - 5.5. Prüfung der Störfestigkeit gegen transiente Störgrößen (Burst) (EN 61000-4-4)
   - 5.6. Prüfung der Störfestigkeit gegen Stoßspannungen (Surge) (EN 61000-4-5)
   - 5.7. Prüfung der Störfestigkeit gegen leitungsgeführte Störgrößen (EN 61000-4-6)
   - 5.8. Prüfung der Störfestigkeit gegen Magnetfelder mit energietechnischen Frequenzen (EN 61000-4-8)
6. Ergebnisse der Einzelprüfungen
   - 6.1. Störaussendung
   - 6.2. Störfestigkeit nach IEC 61000-4-2
   - 6.3. Störfestigkeit nach IEC 61000-4-3
   - 6.4. Störfestigkeit nach IEC 61000-4-4
   - 6.5. Störfestigkeit nach IEC 61000-4-5
   - 6.6. Störfestigkeit nach IEC 61000-4-6
   - 6.7. Störfestigkeit nach IEC 61000-4-8

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Entwicklungs-/ Fertigungsunterlagen nach DIN/EN/ISO 9000ff.

- **Vollständiger „Design History Record“ vorhanden**
  Berechnung , Simulation / Entw.-Dokumentation / Lieferantenverweise / Revisionsdienst
- **Ausgangskontrolle**
  Individuelles Detektor-Prüf-Protokoll / Test Schaltschrank nach VDE 0711/12 (Protokoll)
- **Umfangreiche Software-Dokumentation**
  Interne und externe Dokumentation / Betreiber steht im Blickpunkt

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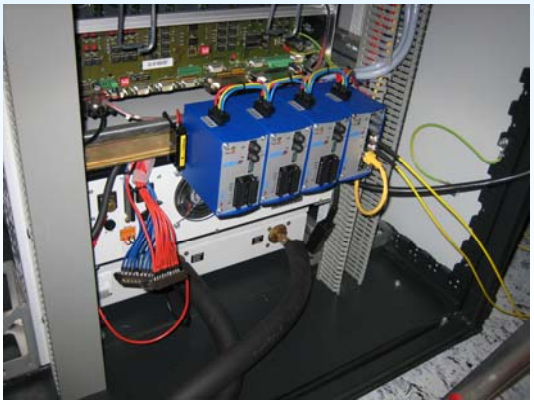
Schaltschrankbau

➔ **Keine Qualitätskompromisse**
Konzept / Aufbau / Zugänglichkeit / Sicherheit

➔ **Schlüsselfertiges QD-System**
Aus einer Hand / ein Ansprechpartner

➔ **Fertigungserfahrung**
Ende 07/2008 160 Detektoren gefertigt



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Ausblick

- **Komplettierung W7-X**

  Fertigung von weiteren 420 - 600 Detektoren + Racks + Schaltschränke
  Erweiterung Remote-Schnittstelle für WinCC®-Anbindung

- **EU: Bedarf bei ITER ca. 1000 Quench-Detektoren**

  IPE-QD-System besitzt viele Detaillösungen
  Sicherheitsmassnahmen auf höchstem Niveau
  Einhaltung aller relevanter Normen

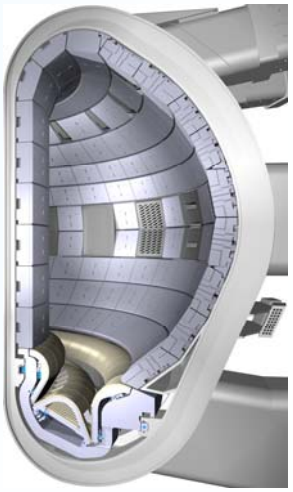
ITER-Anforderungen:

(Geringfügig) höhere HV-Anforderungen
Sprachanforderungen (engl., franz.)

Vorteilhaft:
U_L-Listing (Underwriters Laboratories), CSA

Für Aquisition wichtig:

➔ **Werbung**



Schnittbild Toroidalspule

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Vielen Dank für Ihre Aufmerksamkeit !

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Batterie - Management für Lithium-Ionen Akkus

Forschungszentrum Karlsruhe

Institut für Prozessdatenerfassung und Elektronik (IPE)

K. Schlote-Holubek

Batterie - Management für Li-Ionen Akkus

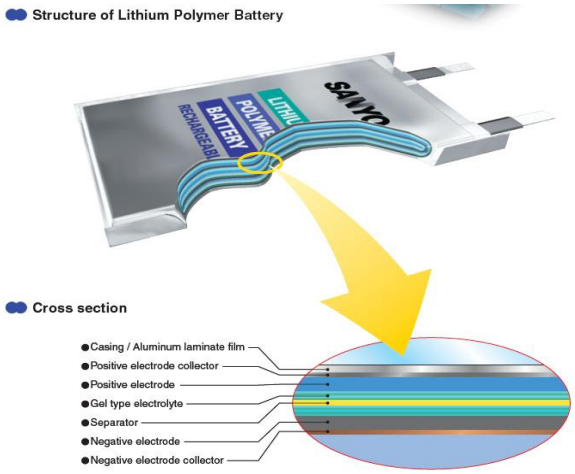
- **Aufbau von Lithium-Ionen Akkus**
  - Bauformen, Materialien, Chemikalien
  - Eigenschaften
  - Sicherheit, aktiv – passiv
- **Aufgaben eines Batterie - Managementsystems**
  - Smart Battery Standard (SBS)
  - Verfügbare Systemtechnik
  - Komponenten (Lader, Monitoring, Balancing, Füllstand)
  - Prinzipaufbau
- **Anwendungen im IPE**
- **Beispiel Teslar Roadster**
- **Zukunft Aussichten**

Batterie - Management für Li-Ionen Akkus

Aufbau von Lithium-Ionen Batterien

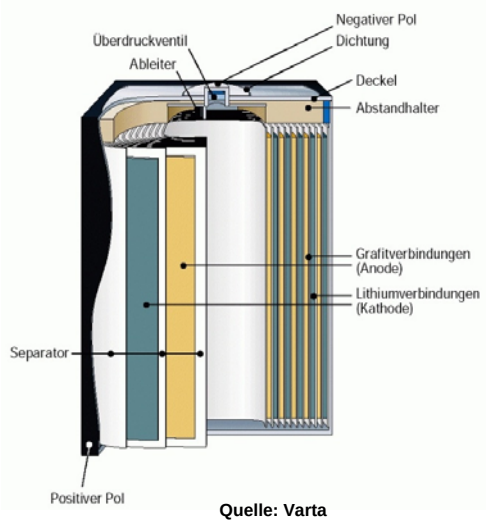
Bauformen

Lithium Polymer Zelle



Quelle: Sanyo

Rundzelle



Quelle: Varta

Batterie - Management für Li-Ionen Akkus

Aufbau von Lithium-Ionen Batterien

Materialien, Chemikalien

- **Anode**
  - hauptsächlich Graphit (z.Zt. Standartmaterial)
  - nanokristalines Silizium
  - Lithium Titanat
- **Kathoden**
  - Lithium-Kobaltoxide (120-130 Ah/kg, giftig, weit verbreitet)
  - Lithium-Nickeloxid (120-150 Ah/kg, 3,6 V, keine Hochleistungszellen möglich)
  - Lithium-Eisen-Phosphat (bis 3kW/kg 35-100C Entladeströme möglich, eigensicher, 3,3V)
- **Elektrolyt**
  - Mischung aprotische Lösungsmittel wie Ethylencarbonat mit dünnflüssigen Alkylcarbonaten (z.B Dimethylcarbonat) und Leitsalz Hexafluorphosphat LiPF6 (leicht brennbar, HF)
- **Separator**
  - Nanoporöse Folien,
  - Neuentwicklungen auf Vliesbasis mit Keramikoberfläche (Leistundsdichte der Zelle)

Batterie - Management für Li-Ionen Akkus

Energie und Leistungsdichte

Akku	U_{Zelle}	Spez. Energie	Spez.Leistung
Blei-Bleidioxid	2,1 V	30-35 Wh/kg	50-100 W/kg
Nickel-Cadmium	1,3 V	45-50 Wh/kg	150-200 W/kg
Nickel-Metallhydrid	1,3 V	50-70 Wh/kg	100-150 W/kg
Li-Ionen-Akku	3,6 V	100-140 Wh/kg	100-200 W/kg
Li-Polymer-Akku	3,7 V	140-150 Wh/kg	200-300 W/kg

Batterie - Management für Li-Ionen Akkus

Eigenschaften von Li-Ionen-Akkus

Zellenspannung zwischen 2,5 V und 4,2 V muss strengstens eingehalten werden! (+/- 50 mV) – Je nach verwendetem Kathodenmaterial variieren die Spannungsgrenzen

Temperaturbereich: 0° C bis max. 75 °C (Ideale Betriebstemperatur zwischen 18 °C und 25 °C)

Kein Memoryeffekt (Flaches Zyklen ist sogar vorteilhaft für die Akkuzelle)

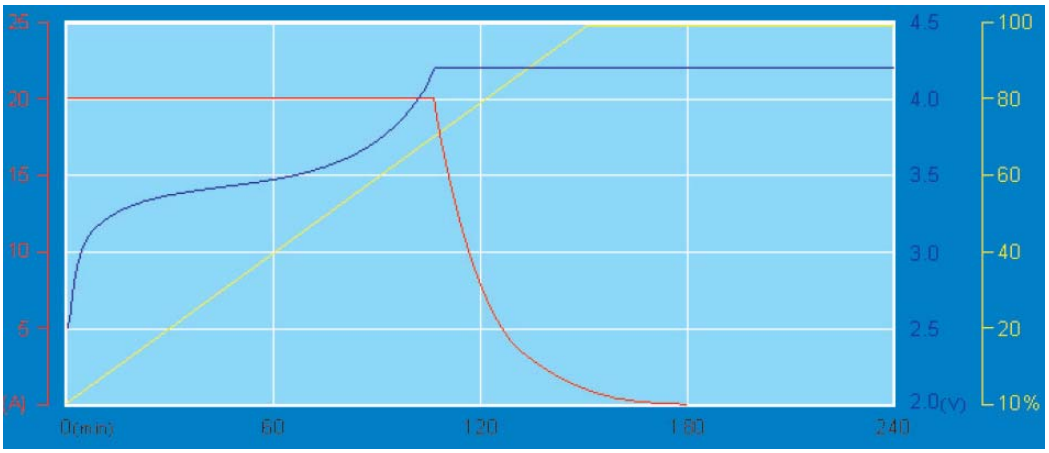
K. Schlote-Holubek

KIT – die Kooperation von Forschungszentrum Karlsruhe GmbH und Universität Karlsruhe (TH)

Forschungszentrum Karlsruhe in der Helmholtz-Gemeinschaft

Batterie - Management für Li-Ionen Akkus

Eigenschaften von Li-Ionen-Akkus



Ladekurve einer Li-Ionen Zelle mit CC/CV Verfahren

Blau: Spannung

Rot: Strom

Gelb: Kapazität

Batterie - Management für Li-Ionen Akkus

Sicherheits- und Schutzmassnahmen

Quelle: Kroll Ontrack

- **Passive**
  - Überdruck, Schmelzsicherung
  - (in der Zelle integriert)
- **Aktiv** (Elektronische Überwachung)
  - Temperaturen
  - Kontrolliert Lade und Entladevorgänge
  - Load-Balancing
  - Über- und Unterspannung
  - Erkennung defekte Zellen

K. Schlote-Holubek

KIT – die Kooperation von Forschungszentrum Karlsruhe GmbH und Universität Karlsruhe (TH)

Forschungszentrum Karlsruhe in der Helmholtz-Gemeinschaft

Batterie - Management für Li-Ionen Akkus

Aufgaben eines Batterie - Managementsystems für Li-Ionen Akkus

- **Überwachung der Betriebzustände des Batteriesystems**
  (bis zur Einzelzelle)
- **Steuert und Überwacht Lade- und Entladevorgänge**
  (Ladestrom, Load Balancing…)
- **Erkennt kritische Zustände, Einleitung von Maßnahmen**
  (Kühlung, Stromreduzierung, Abschalten…)
- **Kommuniziert mit übergeordneten Systemen z.B. Ladestationen, Verbraucher**
  (Füllstand, Zustände…)

Ziel: Sicherheit, Lebensdauer und maximale Leistung

Batterie - Management für Li-Ionen Akkus

Verfügbare Systemtechnik

Standard: SBS (Smart Battery System Specification)

- wurde von führenden Herstellern für Systemtechnik entwickelt

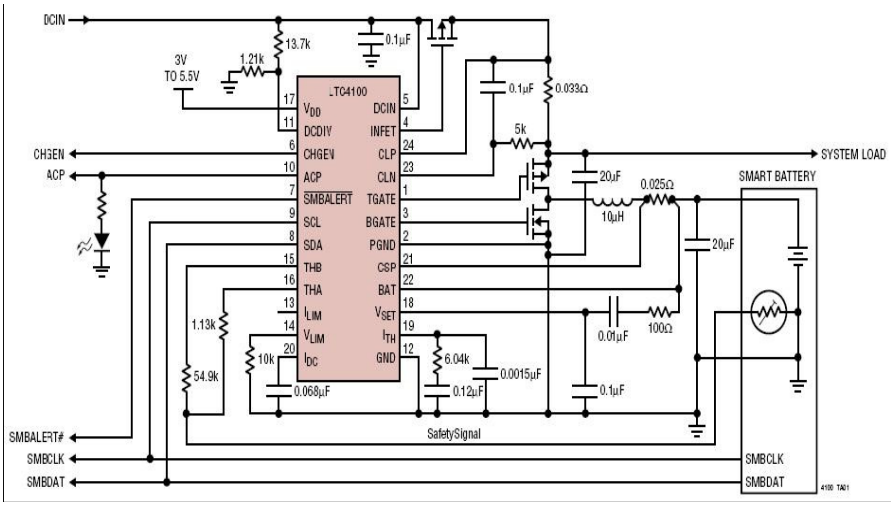
Smart Batteries sind Akkupacks mit interner Schutz- und Überwachungstechnik

- **Charger- Spezification**
  Definition von Eigenschaften, Betriebsmodi und Funktionen von Akkuladern
- **Data- Spezification**
  Beschreibung von SMBus Befehlen (Komunikation zwischen einzelnen Komponenten)
- **Selector- Spezification**
  Beschreibung eines Batterie Managementsystems mit dem mehrere Smart Batteries betrieben werden können

Batterie - Management für Li-Ionen Akkus

Verfügbare Systemtechnik

Blockschaltbild eines Lade- Bausteins nach der Smart Battery Specification

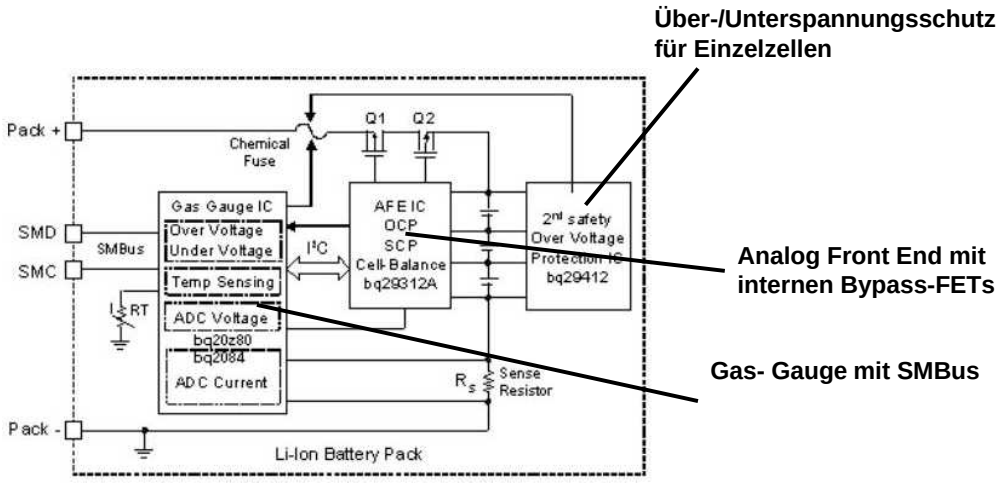


Typische Verschaltung des LTC4100 (Auszug aus Datenblatt von Linear Technology)

Batterie - Management für Li-Ionen Akkus

Verfügbare Systemtechnik

Blockschaltbild eines Gas-Gauge IC`s mit Schutzschaltung, Ladestanderfassung (Gas- Gauge) und Ladestandsausgleich (Load- Balancing) und Temperaturerfassung



Batteriemanagement für Li-Ionen Akkus

Ladestandsmessung (Gas- Gauge)

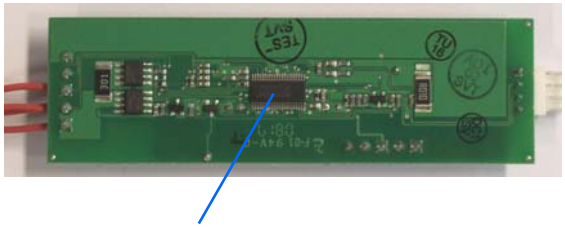
- **Anfangskapazität der Akkuzellen**
- **Über den Betrieb des Akkusystems aufintegrierten Stromverlauf**
- **Entladerate (Dischargerate – Entladestrom)**
- **Temperatur**
- **Zellencharakteristik (Temperatur- und Stromabhängigkeit der Zellenspannung / Zellenimpedanz)**

Die Zellencharakteristik wird vom Hersteller bekannt gegeben oder muss in Eigenarbeit unter festgelegten Testbedingungen gemessen werden und erstellt werden.

Batterie - Management für Li-Ionen Akkus

Verfügbare Systemtechnik

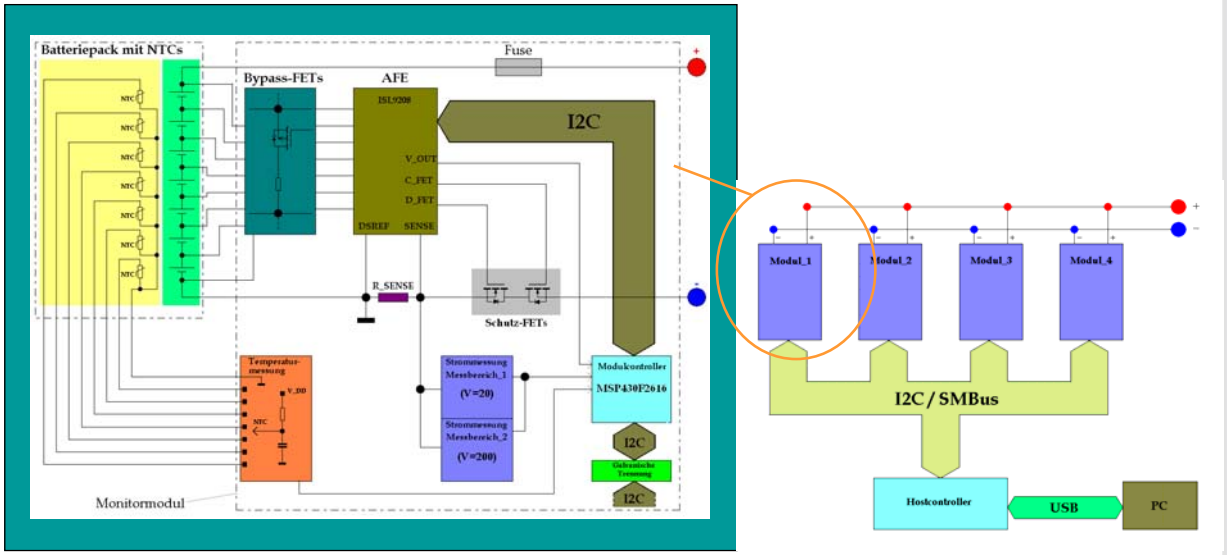
Für die Realisierung von Schutz-/ Überwachungsschaltungen für Li-Ion-Akkusysteme stehen bereits mehrere integrierte Schaltungen auf dem Markt zur Verfügung



BQ20Z95 von Texas Instruments (Hochintegrierter Gasgauge-IC für bis zu 4 in Reihe geschaltete Akkuzellen)

Überwachungs- Analog Front End für bis zu 12 in Reihe geschaltete Akkuzellen von Intersil

Batterie - Management für Li-Ionen Akkus

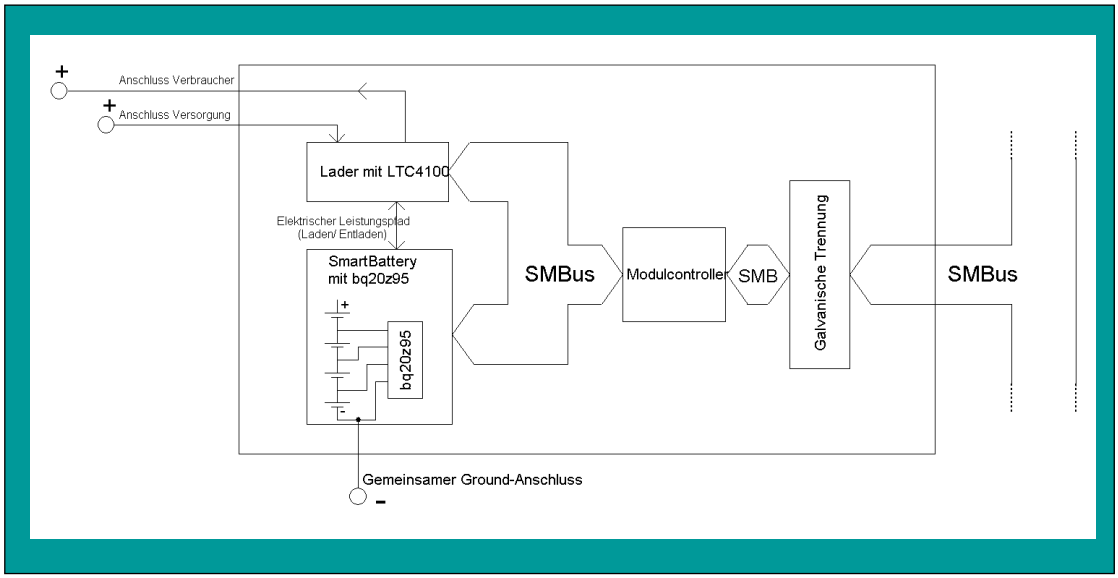


Beispiel einer Lade- und Charakterisierungseinheit mit
-> Temperaturerfassung
-> Stromerfassung
-> Load-Balancing
-> µC basiert (incl. Kommunikation mit PC)
-> Schutzeinrichtungen im Lade/Endladebetrieb

Batterie - Management für Li-Ionen Akkus

Verfügbare Systemtechnik

Integration der Ladetechnik in Akkumodule



Batterie - Management für Li-Ionen Akkus

Aufgaben im IPE

Quelle: PII Pipetronix

Stromversorgung von Pipeline Inspektionsmolchen durch Li-Ionen Akkusystem

z.Zt. Primerzellen im Einsatz

Quelle: FZK

Antenne für „Radio“ zur Detektion von kosmische Schauer

Insellösung

Stromversorgung über Solarpanel und Li-Ionen Akkupack von Frontend, Datentrigger und Funkstrecke

Einsatzort Argentinien

Batterie - Management für Li-Ionen Akkus

www.teslamotors.com

Tesla Roadster

- 100% Elektrofahrzeug mit Li-Ion Batterien
- 0-100km/h in 3.9 sec., Höchstgeschwindigkeit 216 km/h
- 248 PS, Leistungselektronikmodul mit 200kW
- 350 km Reichweite pro Batterieladung
- 3.5 h Batterie-Ladedauer
- umfassendes Sicherheitskonzept für die Batterien

Batterie - Management für Li-Ionen Akkus

www.teslamotors.com

Motor

- Gewicht ca. 50 kg, Wirkungsgrad 85-90%
- Nur der Rotor bewegt sich (bei Verbrennungsmaschinen über 100 bewegte Teile)
- komplexe Ansteuerungs- und Leistungselektronik/Software
- geringer Kühlaufwand, keine Schmierung, kein KAT, Sauerstoffsensoren, keine Abgase, keine Wasserpumpe, ...

→ „einfaches Motorkonzept“

Batterie - Management für Li-Ionen Akkus

www.teslamotors.com

Batterie Pack

- ca. 450 kg, bestehend aus 6800 Einzelzellen des Typs 18650 (d=18mm, l=65mm)
- 375 V nom. U, 533 A max. I, 53 KWh max. Energie (ca. 8 l Benzin), 200 kW elek. Spitzenleistung
- komplexe Sicherheitstechnologie auf Zellenebene, Modulebene und im gesamten Batterieblock
- Kühlung des Batterieblocks mit Wasser/Glykol-Gemisch
- Kapselung der Einzelzellen in Stahlbehältern

→ „aufwendiges Batteriekonzept“

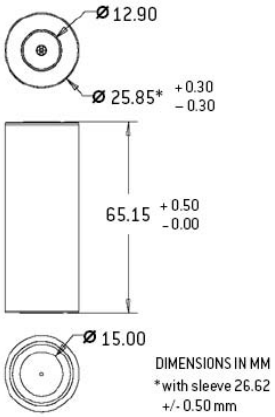
Batterie - Management für Li-Ionen Akkus

Neuentwicklungen

High Power Lithium Ion ANR26650m1

A123Systems' lithium ion rechargeable ANR26650m1 cell is capable of very high power, long cycle and calendar life, and has excellent abuse tolerance due to its use of patented Nanophosphate™ technology.

Nominal capacity and voltage	2.3 Ah, 3.3 V
Internal impedance (1kHz AC)	8 mΩ typical
Internal resistance (10A, 1s DC)	10 mΩ typical
Recommended standard charge method	3A to 3.6V CCCV, 45 min
Recommended fast charge current	10A to 3.6V CCCV, 15 min
Maximum continuous discharge	70A
Pulse discharge at 10 sec	120A
Cycle life at 10C discharge, 100% DOD	Over 1,000 cycles
Recommended pulse charge/discharge cutoff	3.8V to 1.6V
Operating temperature range	-30°C to +60°C
Storage temperature range	-50°C to +60°C
Core cell weight	70 grams



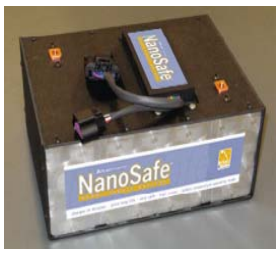
A123Systems
321 Arsenal Street, Watertown, MA 02472
www.a123systems.com

Batterie - Management für Li-Ionen Akkus

Neuentwicklungen von Li-Ion-Akkus erreichen Leistungsdichten von bis zu

4000 W/kg 5000 W/Liter

- **Long life – potentially up to 20+ year life**
- **Very fast charge - rechargeable in minutes**
- **Extremely wide operating temperature range from -50°C/-60°F to +75°C/165°F**
- **Inherent safety – no risk of thermal runaway**



Quelle: Altairnano, Nano Safe

K. Schlote-Holubek
KIT – die Kooperation von Forschungszentrum Karlsruhe GmbH und Universität Karlsruhe (TH)
Forschungszentrum Karlsruhe in der Helmholtz-Gemeinschaft

CompactRIO – The Intelligent Reconfigurable I/O Talking LabView, EPICS And Everything Else

Frank Wiedmann, National Instruments Mark Pleško, Cosylab

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Agenda

- LabVIEW – Open Platform from Control to Sensor
- CompactRIO – Architecture and Modules
- EPICS – Integration
- Outlook

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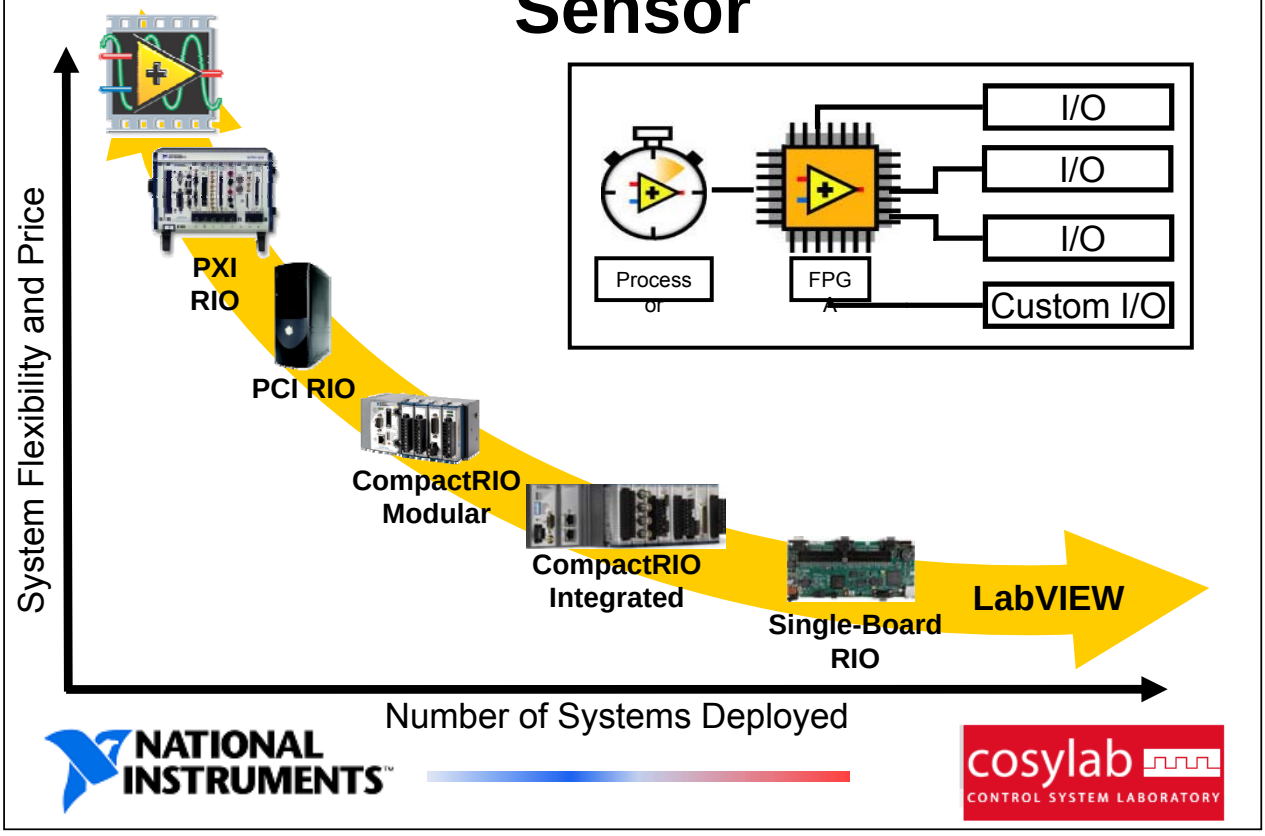
Open Platform from Control to Sensor



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PAC - Systeme

- Vorstellung PAC und ideale Eignung aufgrund Integration komplexer Math

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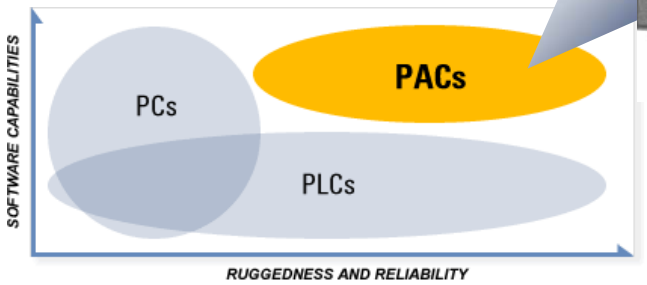
Introduction to CompactRIO

Programmable Automation Controller (PAC)

- **Open Embedded System**
- **Reconfigurable FPGA**
- **Extreme Ruggednes**



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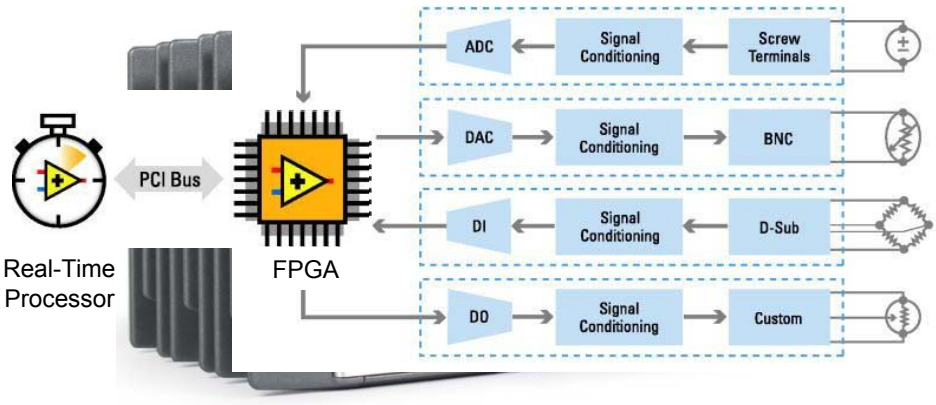
CompactRIO PAC Architecture



- **Real-time processor** for reliable measurement, analysis, connectivity, and control
- **Reconfigurable FPGA** for high-speed and custom I/O timing, triggering, and control
- **I/O modules** with built-in signal conditioning for connection to sensors/actuators

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Building a CompactRIO System

Select the I/O
Analog Input/Output, Digital Input/Output, …
(Low / high speed, simultaneous / multiplexed)

Select the Reconfigurable Chassis
4 slot or 8-slot
1 M Gate or 3M Gate FPGA

Select the Real-Time Controller
400 MHz Pentium Class
64 MB or 512 MB Flash

Select the Connectivity
Standard connector depends on the module
Options: Strain Relief Connector Block, Custom Cable, etc.

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CompactRIO Connectivity Options

10-position screw terminals
(standard on most modules)

cRIO-9932 Strain relief & high voltage connector kit

To meet shock and vibration requirements, you must affix ferrul
to the ends of the terminal wires

cRIO-9935 15-pin Conn. Kit, screw terminals and DSUB s

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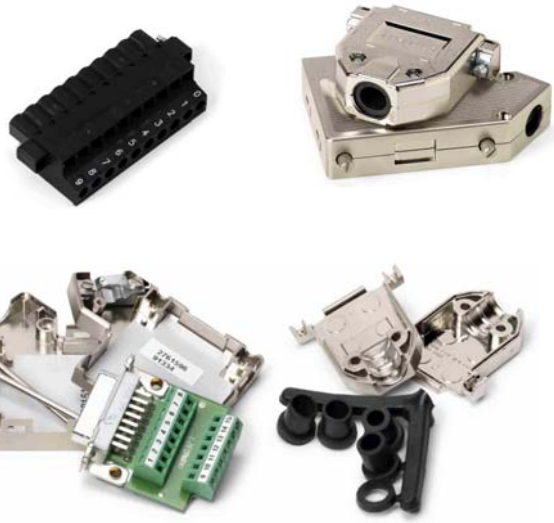
CompactRIO Modules & Connectivity Options

- Voltage Measurements
- Temperature
- Resistance Measurements
- Accelerometers and Microphones (IEPE Sensors)
- Strain and Bridge
- Current Measurements
- Voltage and Current Output
- Digital Input
- Digital Output
- Digital Input/Output
- Relay
- Counter/Pulse Generation
- CAN Communication
- Serial Communication
- Motion
- Removable Storage



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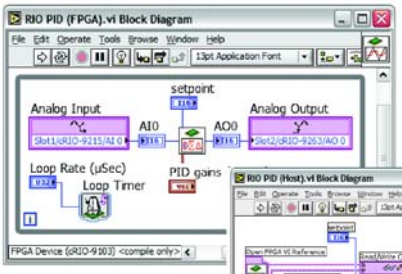
LabVIEW Development with CompactRIO

1. Develop on Host



2. Download to Target

CompactRIO
Real-Time, FPGA Target

3. Deploy to run stand-alone or communicate over Ethernet with host

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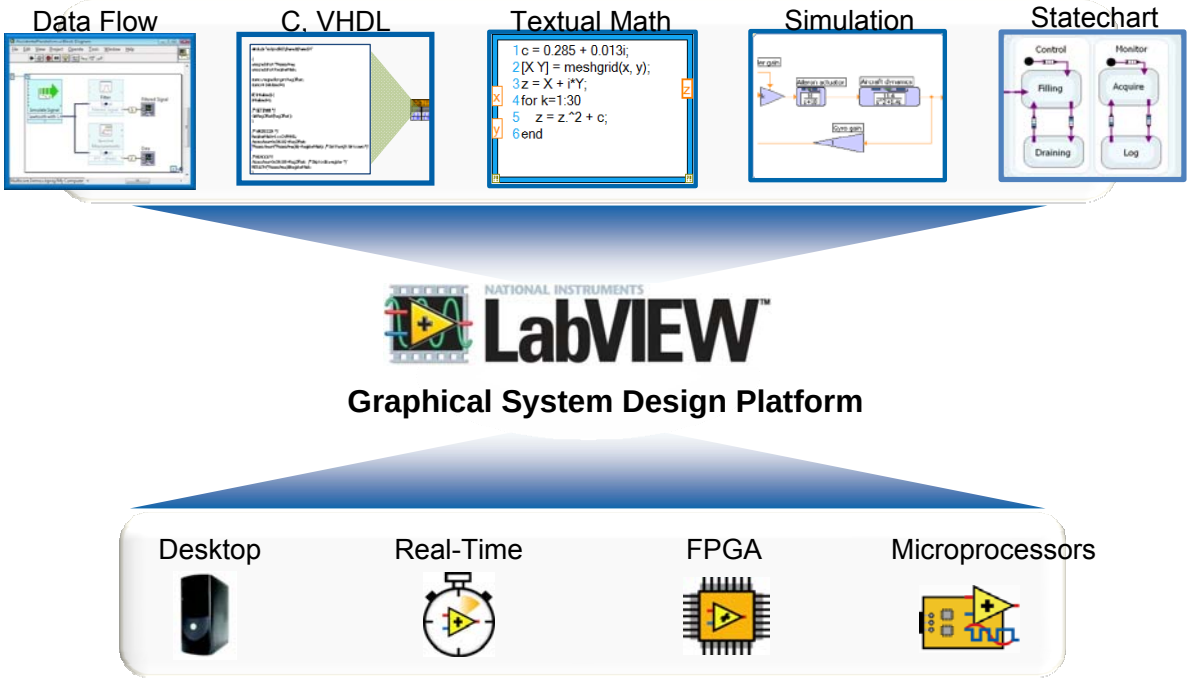
High-Level Design Models



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DISCUSSION (1/2): Are National Instruments FPGAs Really That Useful?

- Take “Off-the-shelf” PXI digitizer boards from National Instruments
- **Add peak detection and coincidence algorithms to onboard FPGA**
  - **Customizable pulse shape recognition parameters**
  - **Preloaded scintillation and solid state detector types**
- Fully integrated into LabView

Model	Resolution (bits)	Sampling (MS/s)	Bandwidth (MHz)	# ch.
5122EX	14	100	100	2
5124EX	12	200	150	2
5922EX	16-24	15	6	2

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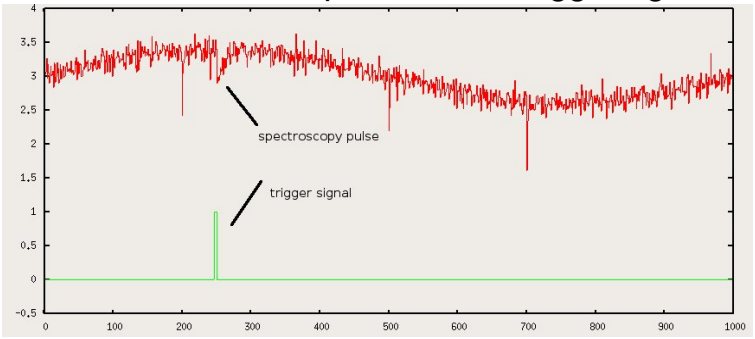
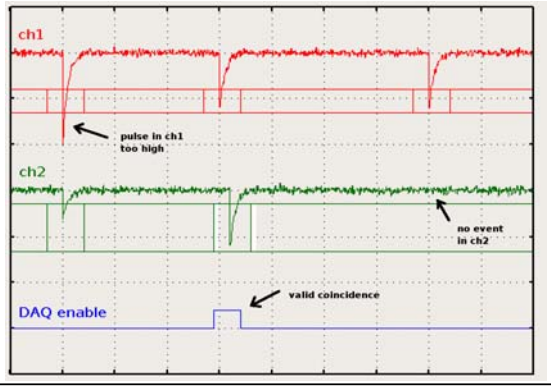
DISCUSSION (2/2): The Short Answer: YES!

- Robust, zero walk, shape-sensitive triggering



- Amplitude-sensitive coincidence or anti-coincidence gated DAQ



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LabVIEW & EPICS ?

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The Challenge of EPICS:
Two Very Different Cultures

- **Device engineers**
  - Want to get things done quickly
  - Many love and use LabView
- **Control system programmers**
  - Need full flexibilty – also at the cost of time
  - Used to their control system package: EPICS, etc.

- The interface must allow both to do their best!
  - Engineers configure and manage device functionality
  - Programmers integrate device into infrastructure (alarm, archive, system administration, maintenance, etc.)

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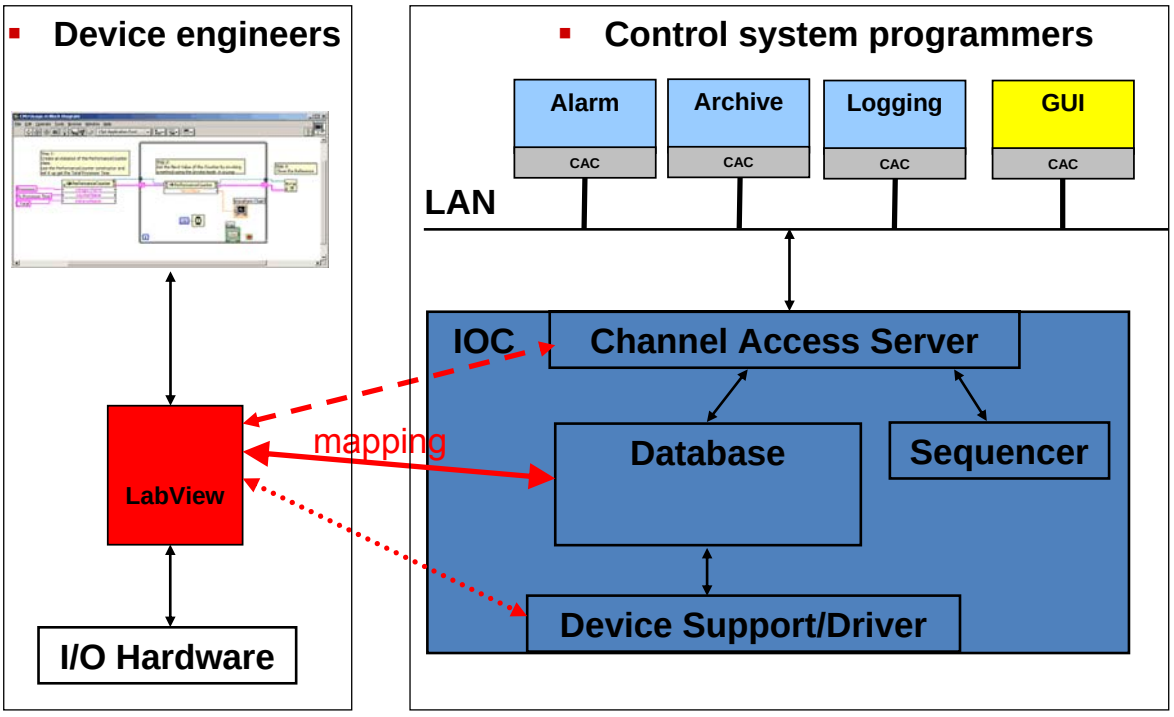
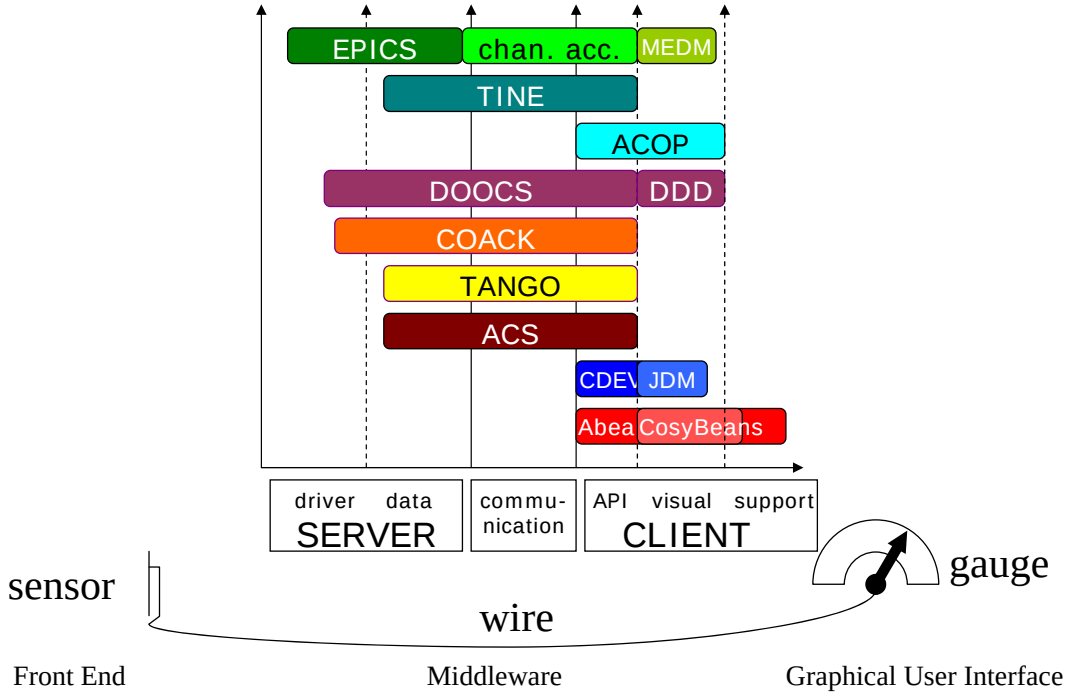
Where to plug?



INTERMEZZO (1/2): What About Other Control Systems?



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INTERMEZZO (2/2): A Control System Is Much More Than Just Middleware

- Control Systems are an **engineering** discipline like all the others, but with an even more complicated cycle
  - Write specifications
  - Architecture
  - Design
  - Prototyping – **probably the only fun part**
  - Test procedures
  - Implementation (coding) – **the only software part**
  - Documentation
  - Testing
  - Debugging
  - Acceptance at customer

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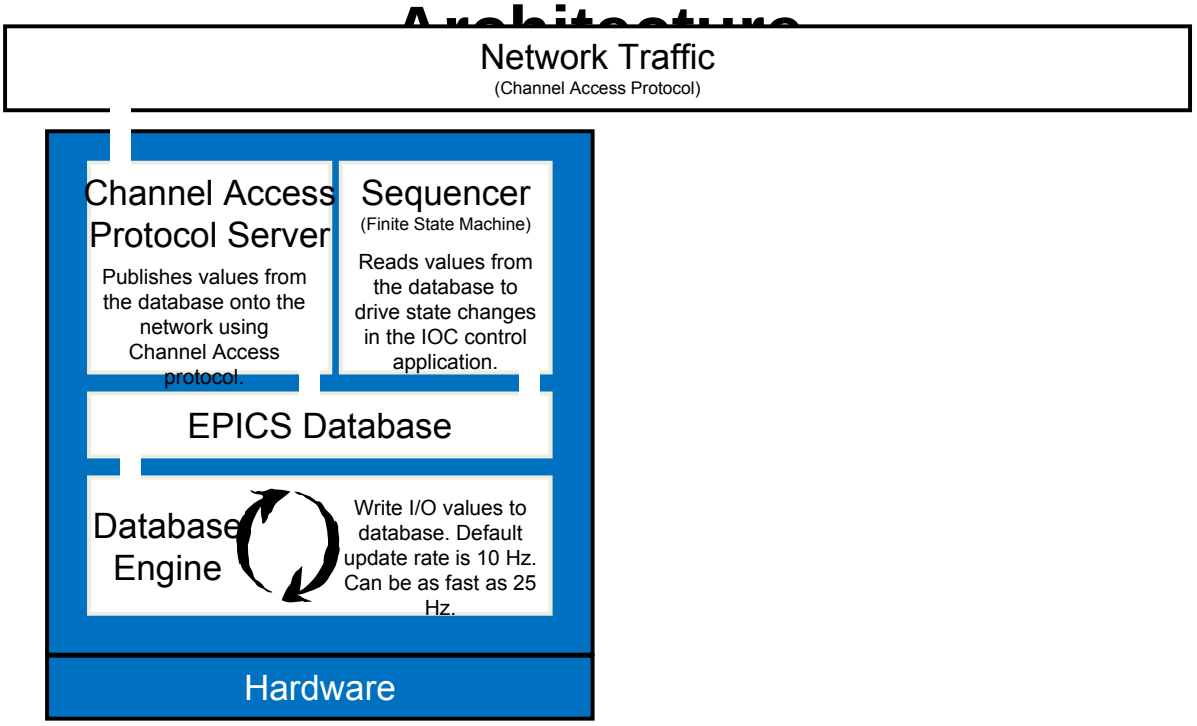
IOC (I/O Controller) SW Architecture



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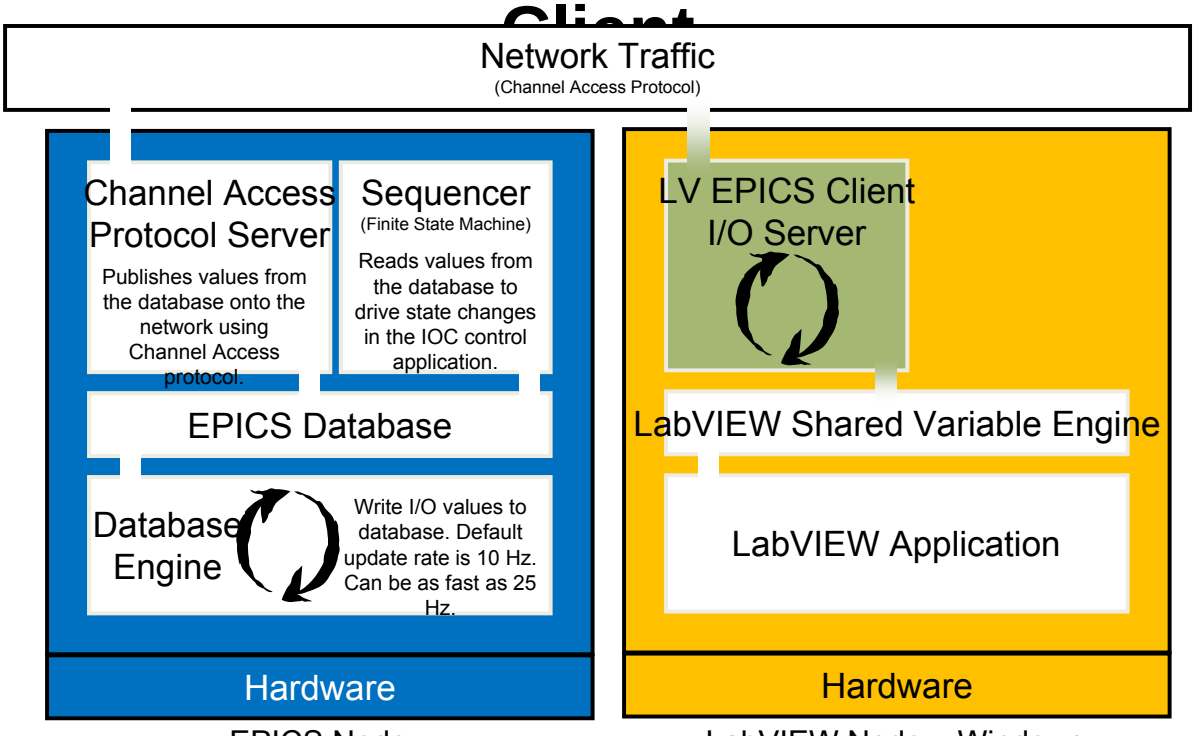
IOC Software with LabVIEW EPICS Client



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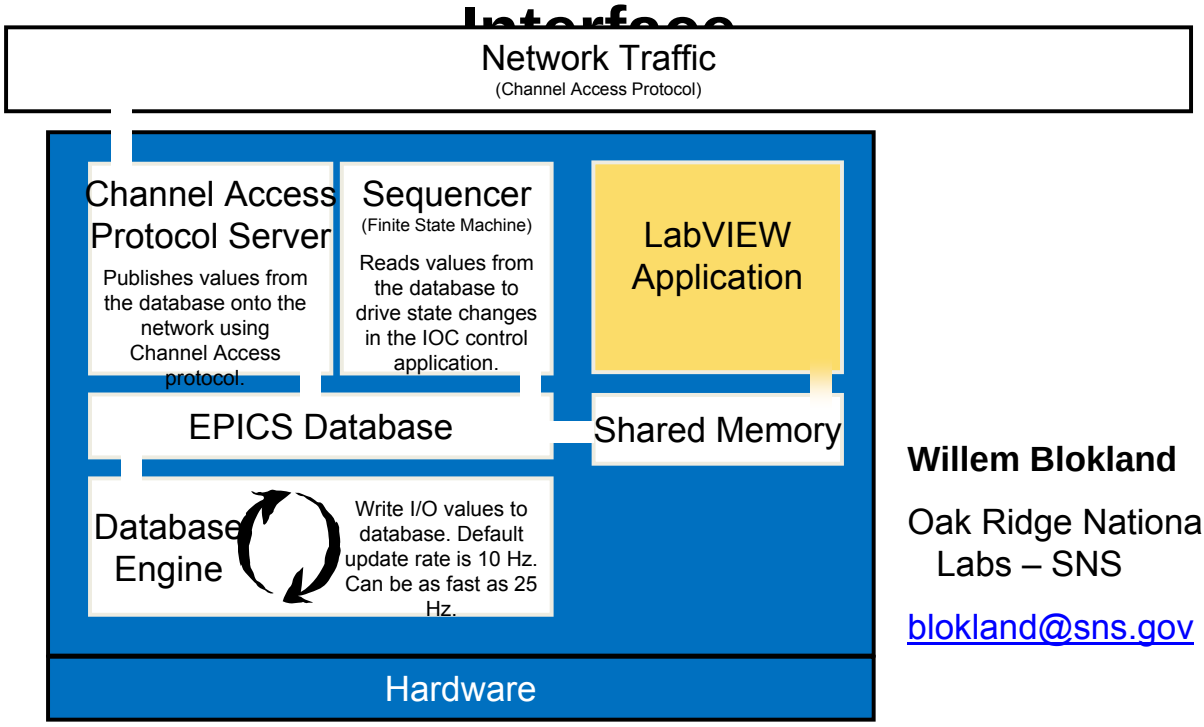
IOC Software with Shared Memory Interface



Willem Blokland

Oak Ridge National Labs – SNS

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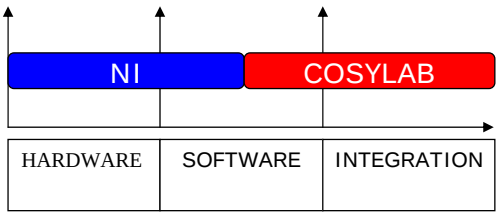
Let's Get Realtime: EPICS on cRIO

- Los Alamos LANSCE-R accelerator upgrade
  - Dilemma: PLC or compact RIO
  - FPGA is a big plus, but need EPICS
- Specific requirements
  - EPICS IOC has to run on cRIO (reuse EPICS software)
  - Graphical programming is required for LV RT and FPGA
  - 2-way communication between EPICS and LV RT
- Challenge: Run LV-RT and EPICS in the same VxWorks process
  - Interthread communication, add NFS and NTP



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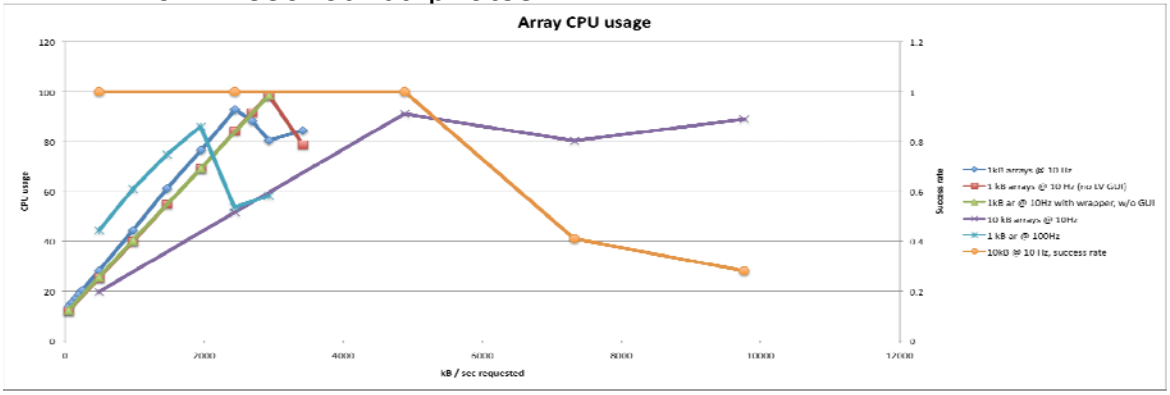
It Works !

- 2-5 MB/sec roundtrip rates



- Open Problems:
  - Mapping of variables between EPICS (records) to LV (VIs)
    - By discipline (naming conventions)?
    - Automatic (two-way generator)?
  - EPICS-LV interference (reboot required for stopping EPICS)

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Let's Go All The Way: cRIO With Any CS On Any OS

- A special cRIO module and PXI card with a separate CPU that separately runs the control system software

- Well defined and supported API to communicate with LV-RT
- Drivers for EPICS, TANGO, TINE, FESA, ACS and others
- **Best of both worlds**:
  - use the power of LV's graphical programming and rich NI hardware family with your favorite control system without having to compromise

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Need Feedback From You: Would You Appreciate Those Benefits Over A Software Solution?

- **Freedom**:
  - use any control system on any operating system
- **Reliability**:
  - CS crash does not affect LV-RT and vice-versa
- **Support**:
  - No grey area with respect to responsibility (LV-RT supported by NI, cRIOC by Cosylab, CS by user)
- **Better performance:**
  - 2 CPUs, no thread races

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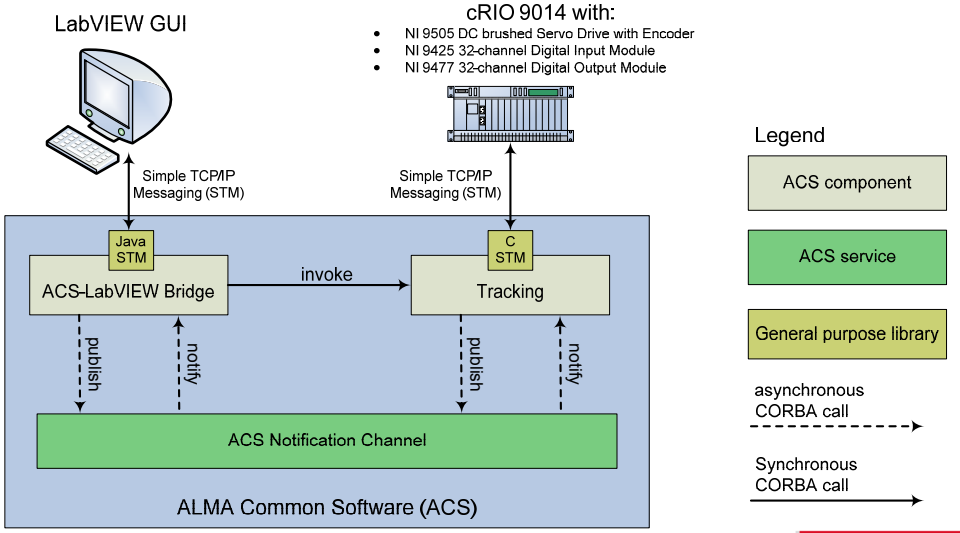
LabVIEW Integration "Für Fortgeschrittene"

- *Extremely Large Telescope* (E-ELT) – a 42m optical telescope
  - Want LV GUI and NI hardware
  - Need ACS as scalable distributed control system infrastructure
- Integration with LabVIEW via *Simple TCP Messaging* (STM)



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Conclusions

- CS packages address different needs than LabView
- LabView can be used with any control system in a clean, open way, getting the best of both systems
  1. “EPICS IOC+LV RT”: make full use of LV RT benefits
  2. Specialized “Control System Connectivity” hardware module
  3. Tunnel LV through control system and “tee” data flow
- National Instuments RIO (FPGA) products have the right flexibility to be enhanced for complex data aquisition
- Cosylab’s system integration expertise brings LabView to any control system in the most efficient way

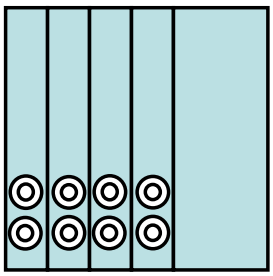
Using Highfrequency Realtime DSOs as Fast Acquisition Systems

LeCroy

Comparison of Systems

Modules

- Samplingrate 8Gs/s /10bit
- Bandwidth 3GHz
- Mudular

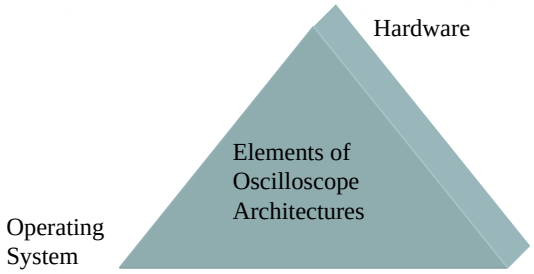


WaveProZi

- Samplingrate 40Gs/s /8bit
- Bandwidth 6GHz (18GHz)
- Data Transfer 250Mpoints/s
- Memory up to 256Mbyte/Ch
- Pre Processing (Software)
- Trigger Pulswidth, Interval etc.,
- Measurement Parameters
  up to 750 measurements /Sec,
  Statistic, Histogram
- Userinterface

LeCroy

WavePro 700Zi Breakthrough Oscilloscope Architecture

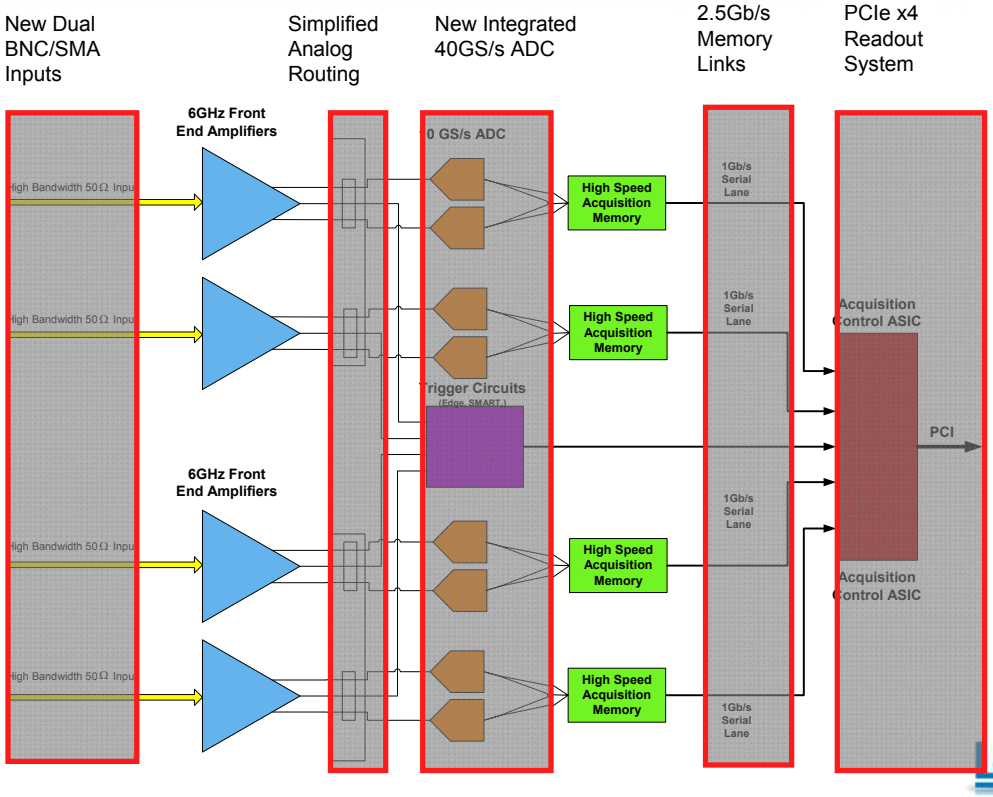


	WavePro 700Zi	Competitors
Processor RAM Waveform Transport	Intel Core 2 Quad 2.5 GHz 8 GB DDR II PCIE x 4	Pentium 4 3.4 GHz 4 GB DDR II PCIE X 1
Operating System	64-bit	32-bit
Processing Method	*X-Stream I I* – variable segment size waveforms sent to cache	Full size waveforms sent to cache

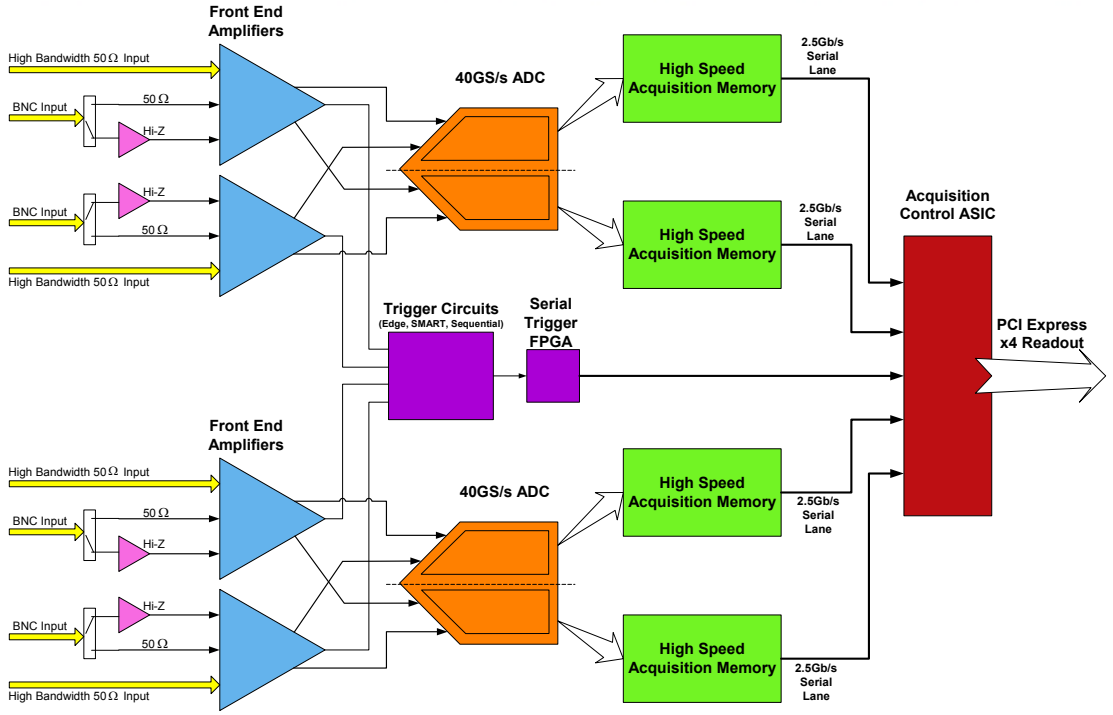
- **All Oscilloscope Architectures Consist of**
  - Hardware
  - Operating System
  - Processing Methodology
- **Traditional Digital Oscilloscopes**
  - Process full size waveforms all in one length
  - Inattentive to CPU-cache architecture
- **LeCroy X-Stream II**
  - Proprietary technology
  - Uses variable waveform segment lengths to ⇨ improve CPU-cache memory efficiency

LECROY X-STREAM II's effective use of cache provides faster processing on long record acquisitions leading to 10-20x greater speeds on long record acquisitions

Improvements from WaveMaster Architecture



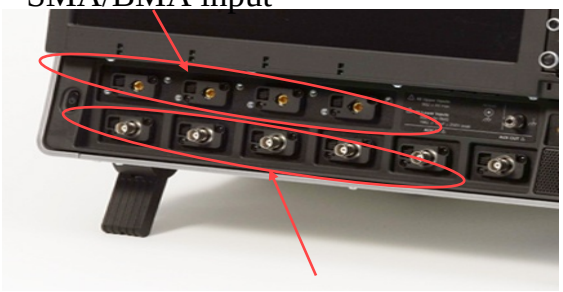
WavePro 7 Zi Hardware Architecture Overview



Dual BNC and SMA Inputs

- High Bandwidth 50 Ω Input
- Wide Dynamic Range 1 MΩ Input
- Use Hi-Z passive probes without adaptors.
- Toggle between SMA and BNC Input without disconnecting input connections

SMA/BMA input



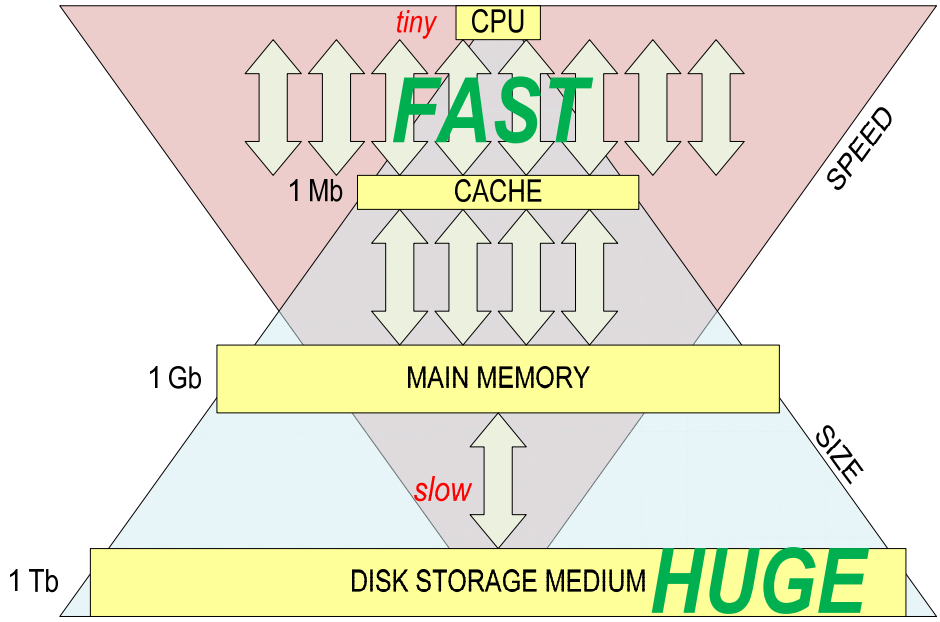
BNC input

	1 MΩ (BNC)	50 Ω (BNC)	50 Ω (SMA)
Bandwidth	**500 MHz**	**3.5 GHz**	**6 GHz**
Risetime	**720 ps**	**120 ps**	**70 ps**
Dynamic Range	**2 mV to 10 V/div**	**2 mV to 1 V/div[1]**	**2 mV to 1 V/div[1]**
Maximum Input Voltage	**±250 V_{pk}**	**±5 V_{rms}**	**± 4 V_{pk}**
Coupling	AC, DC, GND	DC, GND	DC, GND

[1] 2mV-9.99mV/div via software zoom

6

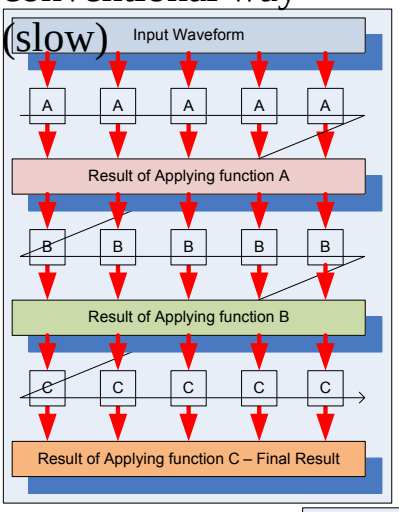
Small Fast Memory vs. Large Slow Memory



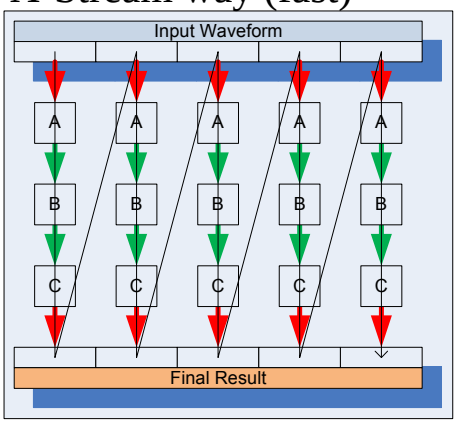
X-Stream I

- **X-Stream processes data in small portions to avoid accesses between cache and main memory.**

conventional way (slow)



X-Stream way (fast)

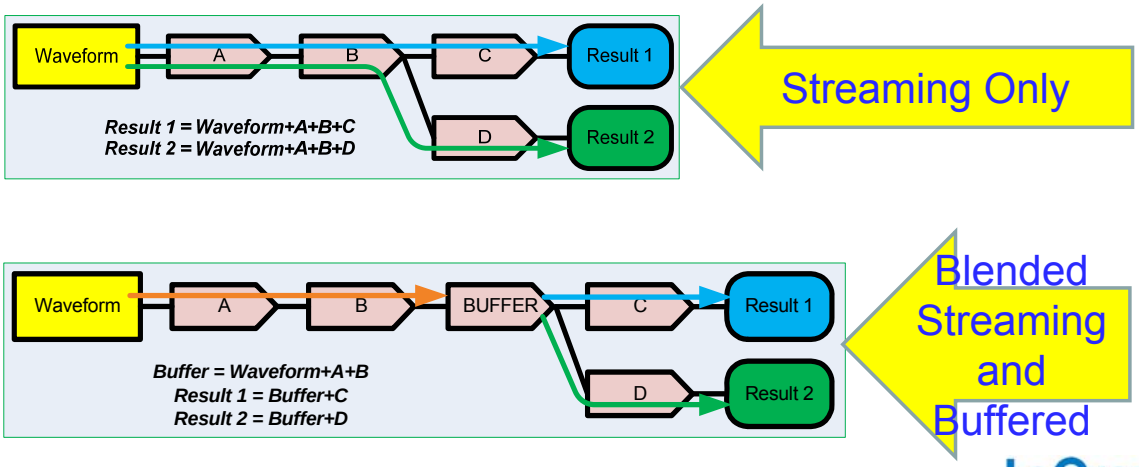


= Operation that results in a "cache-hit" and therefore no main memory access

= Operation that results in a "cache-miss" and/or corresponding main memory access

X-Stream II – Dynamic Buffer Placement

- **Traditional processing has buffers between every processor.**
- **Streaming processing has no buffers.**
- **X-Stream II uses buffers or streaming or a combination depending on which is faster.**



LeCroy confidential 2008

Sequence Mode

- **In sequence mode, the complete waveform consists of a number of fixed-size segments. In sequence mode dead time between trigger events are optimized**
- **Up to 15.000 segments**
- **1,250,000 waveforms/second (in Sequence Mode, up to 4 channels)**

Superior Processing

Math + Histogram + Track	185.000 measurements/sec
FFT (10M Points Waveform)	3.8 Mpoints/sec
Sequence Mode	..
Data Transfer Rate LSIB	250Mpoints/sec

LeCroy

New High Speed Remote Data Transfer System

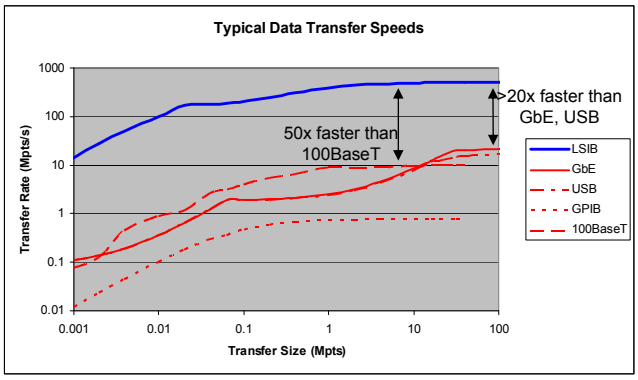
LeCroy

What is LSIB

- **LSIB is:**
  - A new standard for high speed data transfer from the oscilloscope with speeds up to **250MS/s**.
  - Based on the wired **PCI-express** standard.
  - **Unique** to WavePro 7 Zi Series oscilloscopes only.
  - **10x-50x faster** than other instrument control technologies currently available (GPIB, Ethernet, USB, etc.)
  - Primarily intended for **high speed** waveform data transfer from scope to a host computer for off-line processing or storage.

Speed

Code
Great Performance
Some May Need Better
Not Desired



	Time to Transfer Record Length of:		
	1MS	10MS	100MS
GPIB	1 s	10 s	100 s
LAN	0.05 s	0.5 s	5 s
LSIB	0.004 s	0.04 s	0.4 s

- LeCroy's LSIB solution enables data rates up to 250 Mpts/s.
- 10-50x faster than other solutions in use today.
- Uses PCIe x4 bus for remote data transfer.

Comparision LAN / LSIB

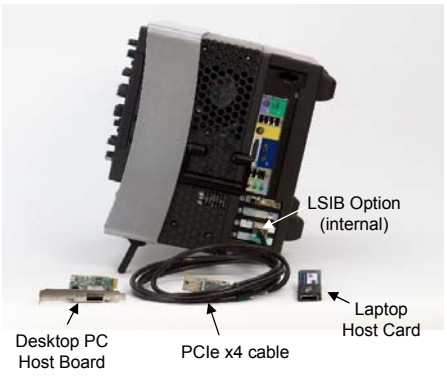
Existing LAN solution

				
Host PC Customer Application, LeCroy IVI drivers, NI-VISA, LeCroy VICP Passport	Interface adapter Ethernet	Bus/Cable LAN cable	Interface adapter Ethernet	Scope XStreamDSO Application

New LSIB Solution

				
Host PC Customer Application, LeCroy IVI drivers, NI-VISA, LeCroy VICP Passport, LeCroy LSIB Driver	Interface adapter LSIB Host card	Bus/Cable PCIe X4 cable	Interface adapter LSIB Device card (Installed in scope with LSIB-1 option)	Scope XStreamDSO Application

Deliverables



- **LSIB-1 Option includes:**
  - PCIe x4 cable
  - LSIB Host card for PC
  - API/Client Software Library
  - LSIB Driver
  - LSIB card installed in scope
- **Customer Requirements**
  - PC that has an extra PCIe slot
  - Programming Capability

LSIB Summary

- Data transfer rate up to **250 MS/s**
- **7 meter** maximum distance between scope and host**.**
- **Geared toward users who need high performance data transfer**
  - Use for high speed off-line data processing or storage.
  - Users need to use the LeCroy provided libraries for developing software applications on their host computers
  - **API/Client Library will be included** for programming LSIB.
- Accepts **legacy** remote commands or **automation** commands
- **Primarily** for **remote data transfer** but can be used for**:**
  - Low Speed Input for control (from host to scope),
  - High Speed Data Output (from scope to host),
  - Bi-directional transfer.

Comparision LAN / LSIB

	LAN		LSIB	
	Input (from host to scope)	Output (from scope to host)	Input (from host to scope)	Output (from scope to host)
Use Case	Receive Commands from Host	Transmit Data to Host	Receive Commands from Host	Transmit High Speed Data to Host
Physical Layer	Ethernet	Ethernet	PCIe x4 bus	PCIe x4 bus
Drivers	IVI Driver	N/A	IVI Driver	N/A
Protocol	TCP-IP protocol	TCP-IP protocol	TCP-IP protocol only	LSIB protocol only
API	NI-VISA+VICP Passport	N/A	NI-VISA+VICP Passport	LSIB API Library only (Not supported by NI-VISA)
Speed	10MS/s	10MS/s	N/A	Up to 250MS/s

FAQ - LSIB

- **Q: Is LSIB supported by NI-VISA?**
  - A: Only for transfer from host to the scope using the VICP passport. LSIB is a custom protocol that is unique to LeCroy and is not supported by NI-VISA for high speed data transfer as of now. LeCroy provides an Client Library and driver for communication with the scope.
- **Q: Is LSIB for data output only?**
  - A: LSIB can also accept remote control commands.
- **Q: Is LSIB backward compatible with my existing test procedures that use the LAN port?**
  - A: LSIB is fully compatible with existing code for LAN to send commands to the scope, but needs additional code to receive high speed data from the scope.
- **Q: Is LSIB reliable and robust?**
  - A: Yes, it is based on the well established cabled PCI-express standard.

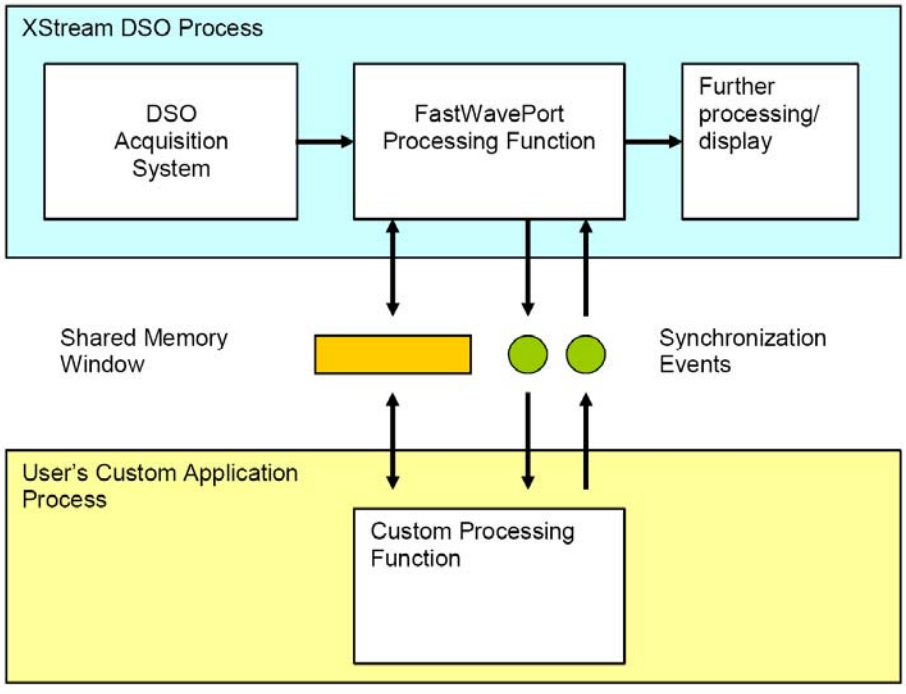
Fast Multi Waveport

FastMultiWavePort

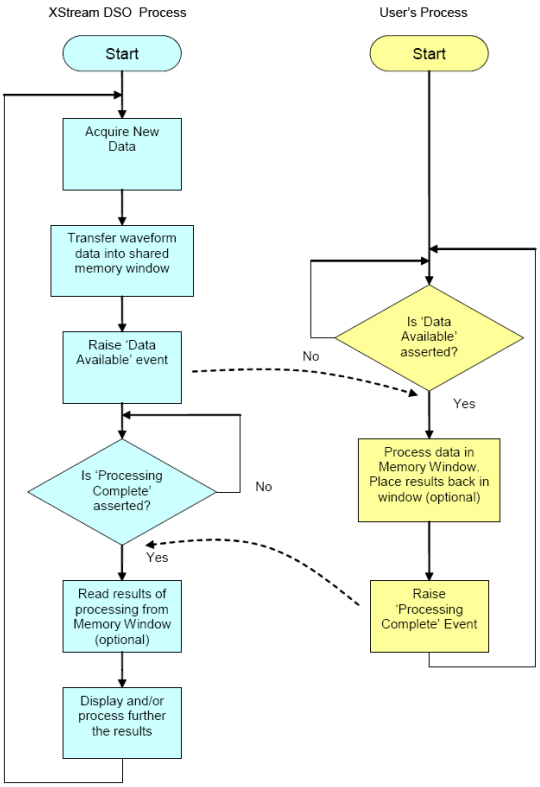
- **FastWavePort is a processing function for the LeCroy XStream Series of Digital Oscilloscopes that enables a user to insert his own custom processing algorithm, written in the C/C++ language, into the DSO's processing stream**

- **For the present two C++ compilers have been tested for compatibility: Microsoft Visual C++ (6.0 to 7.1) and MinGW 'gcc' based compiler (free download from http://www.mingw.org/)**

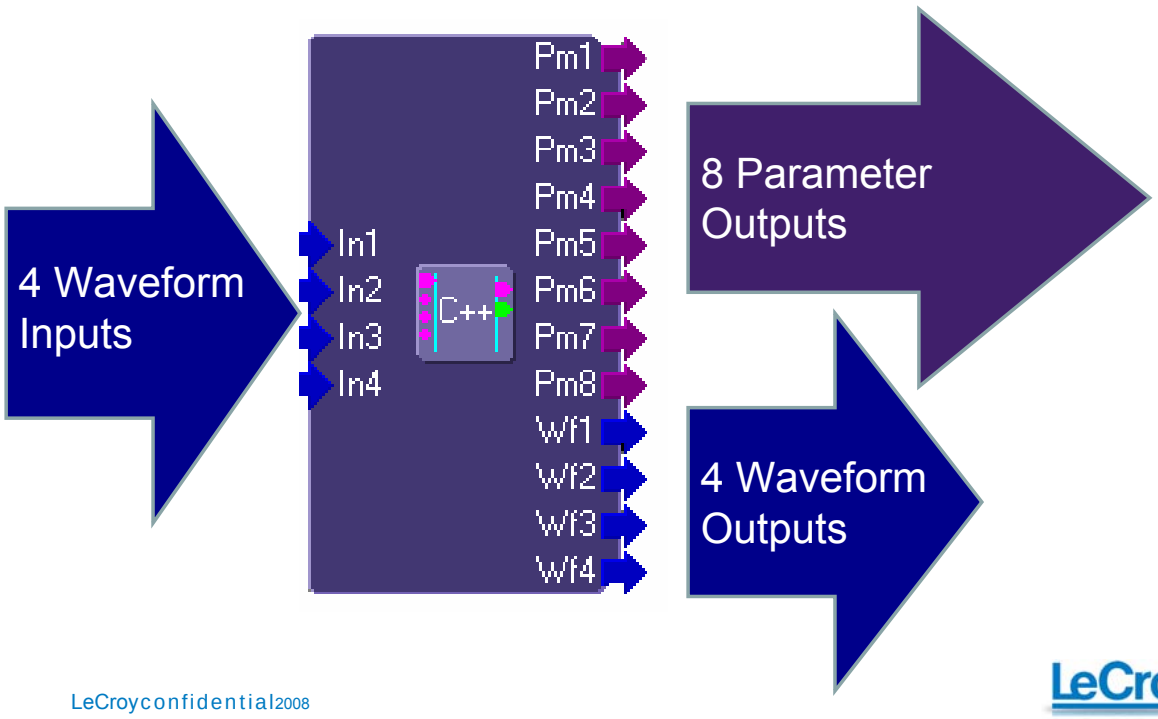
FastMultiWavePort



FastMultiWavePort



FastMultiWavePort



LeCroy confidential 2008

FastMultiWavePort Performance

- **Under optimal conditions, on a DSO with a 1.7GHz Celeron processor, rates of up to 75 MSamples/sec have been observed. Due to the differences between the acquisition and processing hardware in each of the XStream DSOs this value may vary significantly and therefore cannot be guaranteed.**
- **One thing can be guaranteed, this is by far the fastest way to process data using a user-defined algorithm on an XStream DSO.**

SEI Tagung

Greifswald, 23.09.2008

Agenda

- EBV Elektronik
- Altera FPGAs
- EBV Reference Design Example

  Motion Control on FPGA

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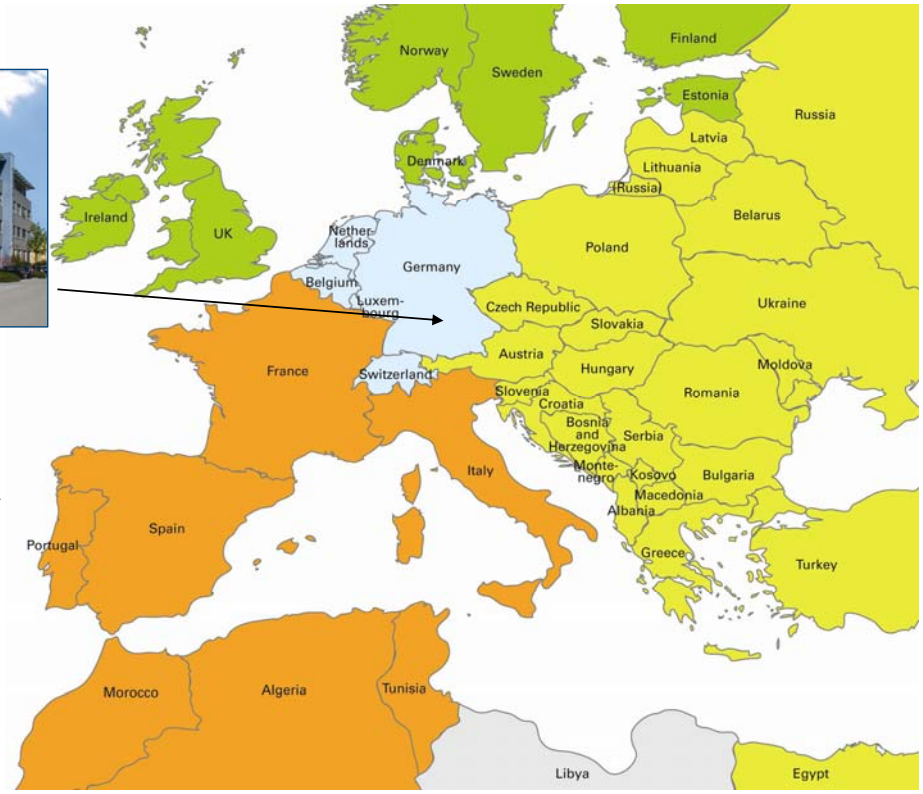
EBV – lokale Präsenz

Europäische Zentrale in Poing bei München

- 59 Büros
- 28 Länder in EMEA



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EBV in Zahlen

- Umsatz: **€ 1,310 Mrd. KJ 2007**
- Mitarbeiter: **908**
- Warenbestand: **€ 260 M**
- Marktanteil: **22.85% Q1 KJ 2008 (DMASS)**

EBV ist zertifiziert nach:

- **EN IEC 61340-5-1 & 2**
- **DIN EN ISO 9001:2000**

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Franchise Partner

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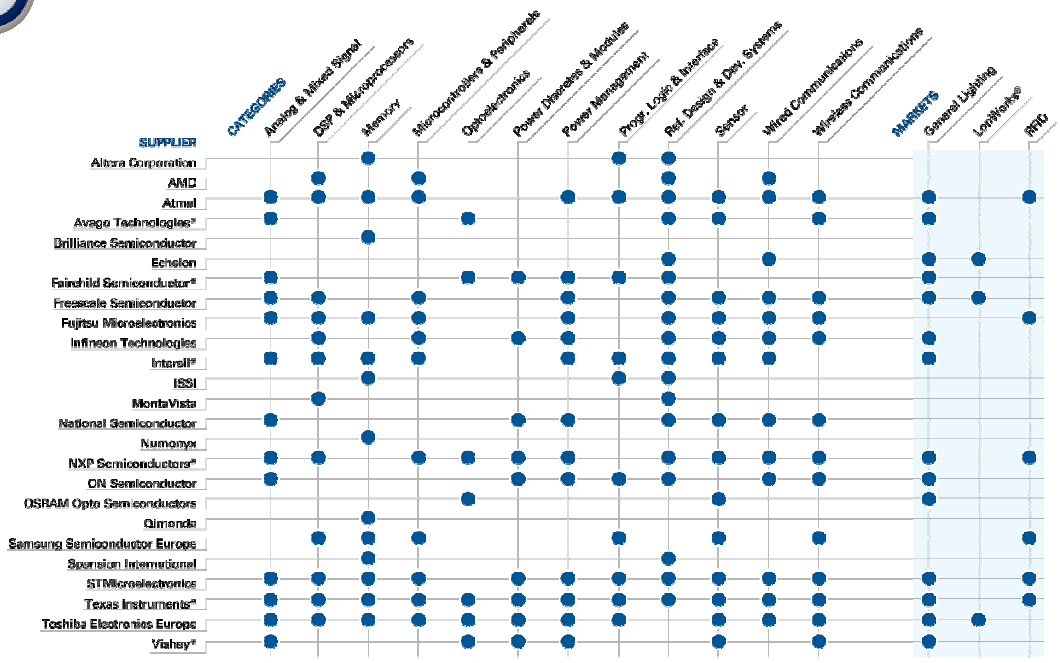
One-stop shopping



*SUPPLIER INFORMATION

- Avago Technologies – Formerly Agilent Technologies
- Fairchild – Acquired Samsung Power Division, Kota Microcircuits, Micro Linear Power Mgmt Division, Intersil Discrete Power Business, Impala Linear Corporation, Signal Processing Technologies, Raytheon
- Intersil – Acquired Elantec, Xicor
- NXP – Formerly Philips Semiconductor
- Texas Instruments – Acquired Burr Brown, Power Trends, Unitrode, Benchmarq, Chipcon
- Vishay – Acquired General Semiconductors

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EBV der technische Spezialist

Design Partner Netzwerk

Engineering Firmen fungieren als Design Partner und bieten technische Unterstützung für sehr komplexe Anwendungen. D.P. konzentrieren sich auf Software- und Hardware-Entwicklung mit Fokus auf DSPs, Power, FPGAs, High-End Processing und Networking.

Kompetenz Teams

Spezialisierte FAEs bieten spezifisches Produkt- und Anwendungs-Know-how für DSPs, programmierbare Logik, Power, Microcontroller, Analog, High-End Embedded Processing, Networking & Telekom, General Lighting, Bluetooth™ & WLAN, Control Networks und Automotive.

Knowledge Base

Eine Online-Datenbank, die innovative Lösungen für komplexe Anwendungen inklusive detaillierter Produkt-Spezifikationen beinhaltet. Minimiert Mehrfachsuche bei identischen Designs und verringert dadurch entscheidend Kosten und Time-to-Market.

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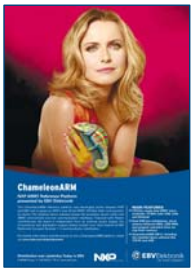
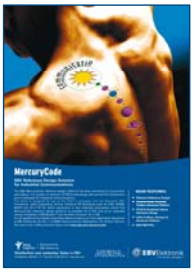
EBV Referenzdesigns

- Start des Programms in Q4 2006
- Mehrere Hersteller auf einer Lösung
- Neueste Produkte, Technologien & Software
- Kundenbedürfnisse treiben die Anwendungen
- EBV definiert die Zusammenstellung
- Eins-zu-eins-Umsetzung möglich
- Spart Kunden Kosten und Entwicklungszeit
- Verkürzt Time-to-Market





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Produktveredlung 1

Programmierung

- 20 automatische Programming-Pick & Place-Maschinen
- 12 automatische Programming-Serial-Handlers
- 5 Media-Transfer-Systeme mit 3D-Lead/BGA-Inspection
- Manuelle Programming-Maschinen
- 5 Laser-Marking-Systeme
- Peel-Strength-Analyse
- Component Screening
- Vakuum-Ofen für Baking
- Dry-Packing nach JEDEC

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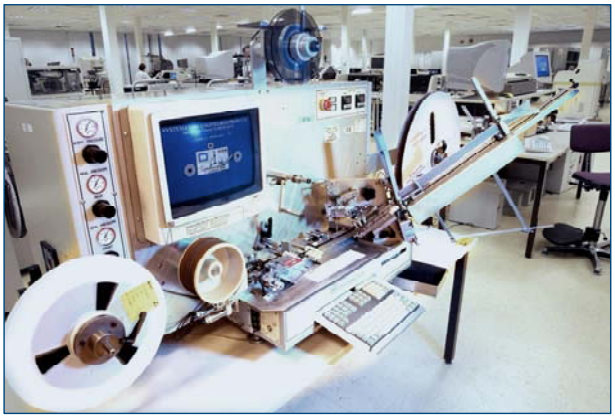
Produktveredlung 2

Tape & Reel

- EBV bietet Tape & Reel auch als separaten Service
- Kapazität von über >40 M Bauteilen pro Jahr garantieren ausreichende Flexibilität
- Alle Materialien und Abläufe nach EIA481 Standards
- Peel-Force-Test für jedes Tape dokumentiert
- 60% der programmierten Bauteile sind gegurtet



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Produktveredlung 3

Laser Marking

- Schnell, flexibel und unkompliziert
- Hitzebeständig
- Maschinelles Handling garantiert hohe Qualität
- Hohe Kosteneffizienz

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Altera FPGAs

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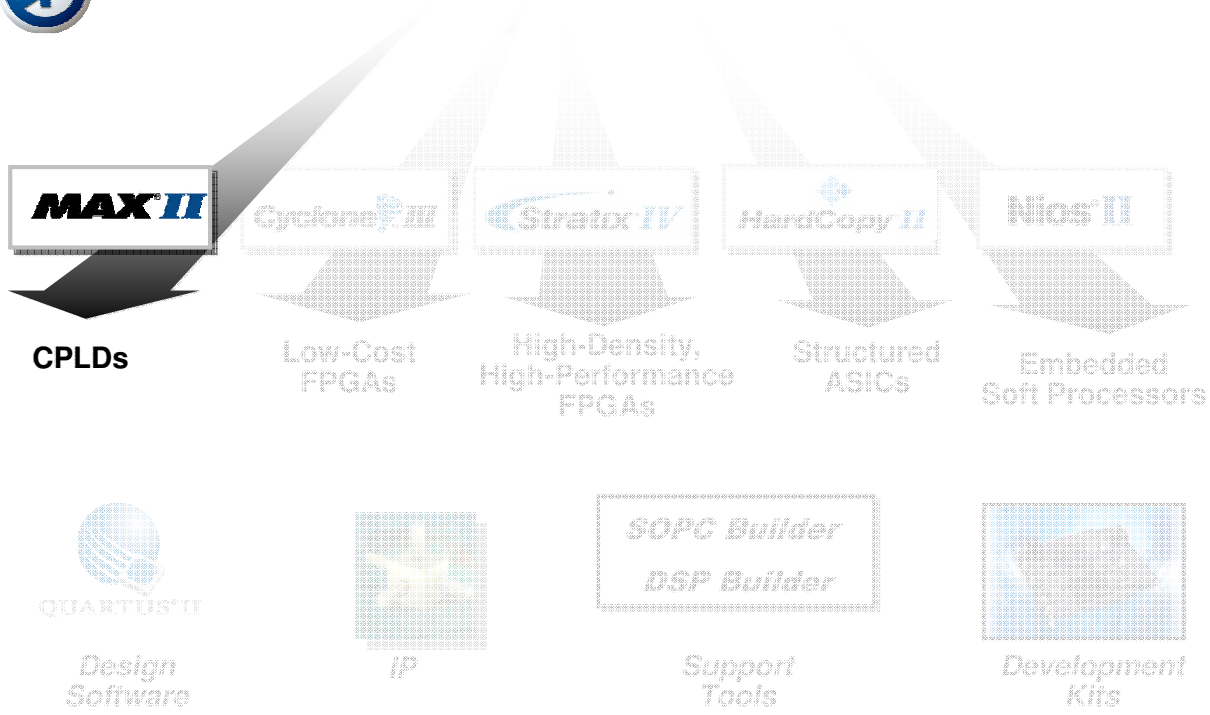
A Complete Solutions Portfolio



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MAX II: The Lowest-Cost CPLD Ever

- New logic architecture
  - 1/2 the cost
  - 1/10 the power
  - 2X the performance
  - 4X the density
- Non-volatile, instant-on
- Supports 3.3-, 2.5-, and 1.8-V supply voltage
- Zero Power devices Available

Breakthrough Technology to Expand the Market

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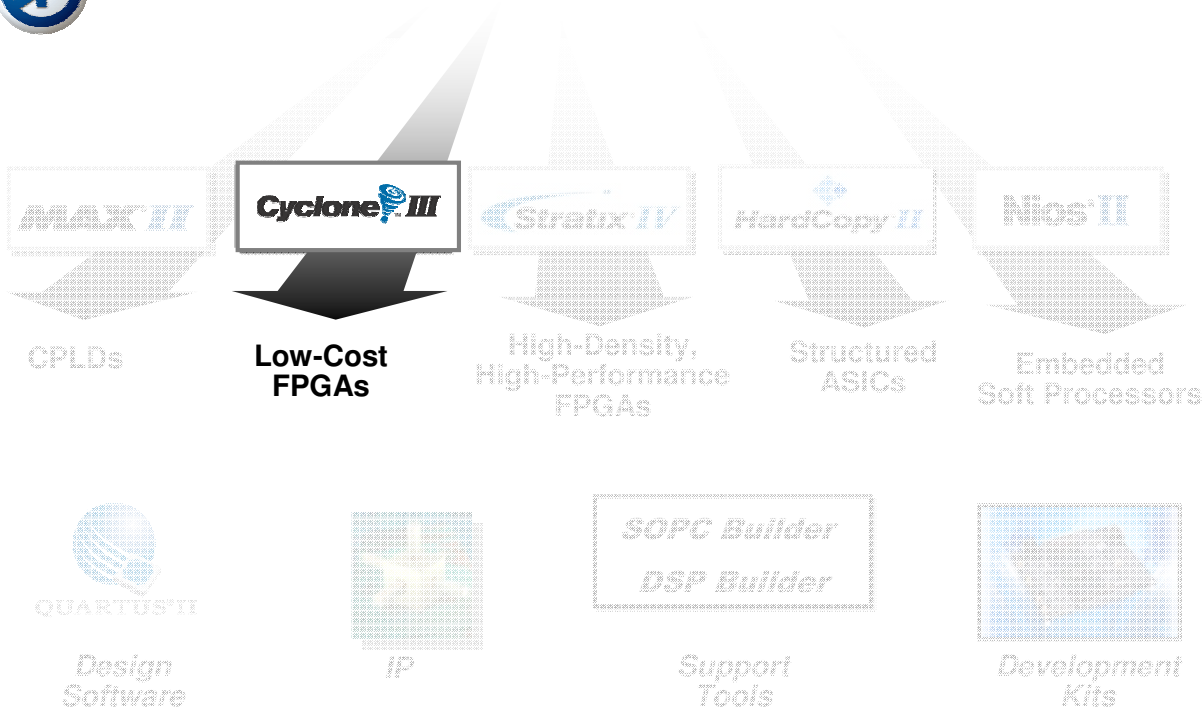

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Unprecedented Combination

- Low power
  - TSMC 65-nm low-power (LP) process
  - Quartus® II software power-aware design flow
  - 120K logic elements (LEs) under ½ W static
- High functionality
  - Densities ranging from 5K to 120K LEs
  - Up to 4 Mbits of embedded memory
  - Up to 288 embedded multipliers for digital signal processing (DSP)
- Low cost
  - First low-cost 65-nm FPGA
  - Free Quartus II Web Edition software

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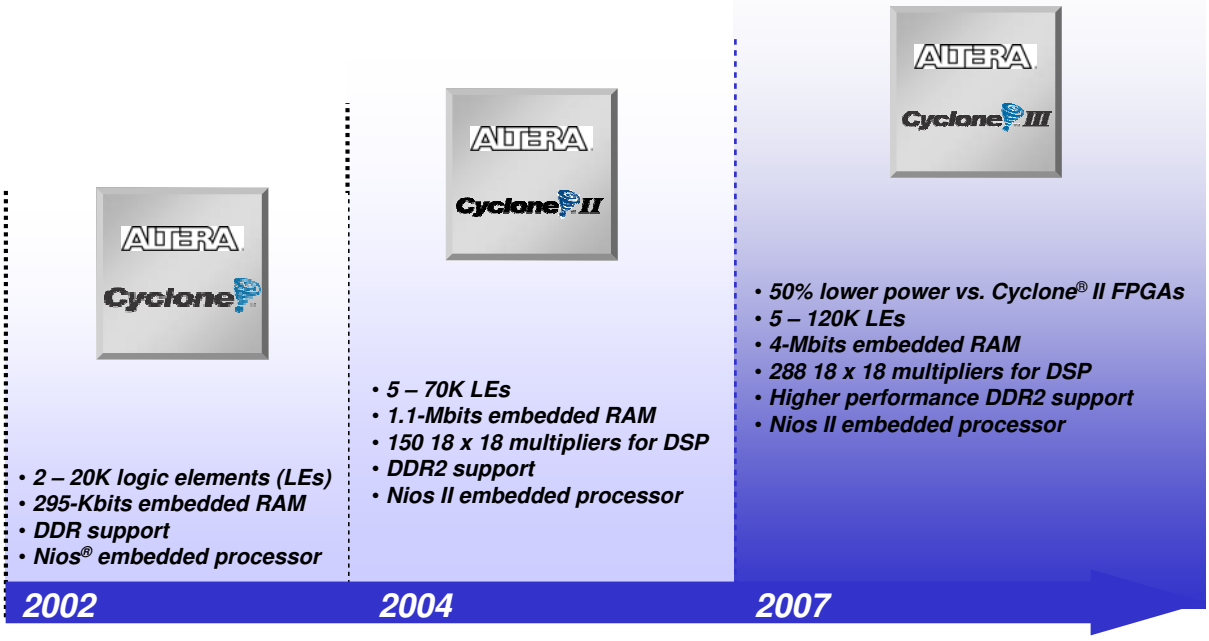
Meeting the Needs of emerging high-volume Applications



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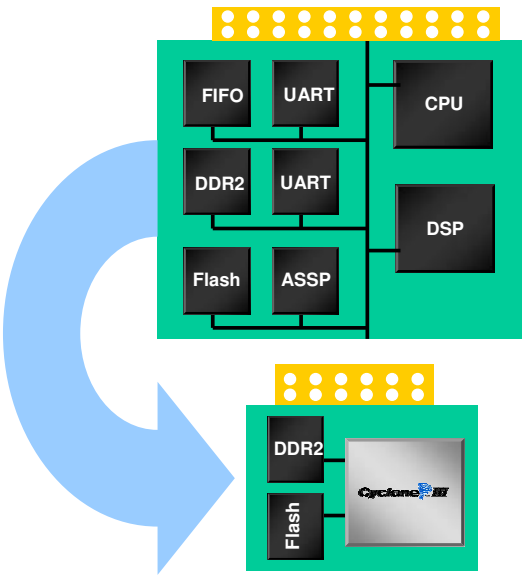
System Integration

- System integration eases your design constraints
  - Board space requirements
  - Cost pressures
  - Product obsolescence concerns
  - Short development times
- Cyclone III FPGAs—complete feature set for better integration over any other low-cost FPGA



Do more with less!

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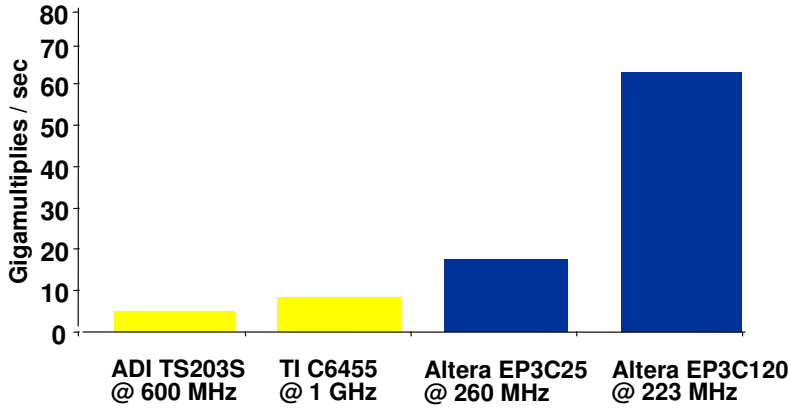
System Integration

- Combination of logic, memory, and multipliers allows for efficient implementation of arithmetic DSP functions
  - Integrate multiple DSP devices into a single Cyclone III FPGA
  - Process multiple signal data streams at lower cost per channel than dedicated DSP devices



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BARCO Media and Entertainment

"In the search to find the ultimate combination of functionality, size, and cost, Barco opted for Altera's Nios II processor implemented in a Cyclone device after it became clear that no other processor delivered the ideal mix of features, price, performance, and short time-to-market, along with a guarantee to avoid costly processor obsolescence."

—Robbie Thielemans
Vice President of R&D

Application:

Modular LED Display System

Industry:

Broadcast

Altera Value Proposition:

- ***Accelerated Market Releases with the Most Advanced Video Processing Features***
- ***Cost-Effectiveness and High Volume Availability for Consumer Market***

Altera Products Chosen:

Cyclone

Nios II

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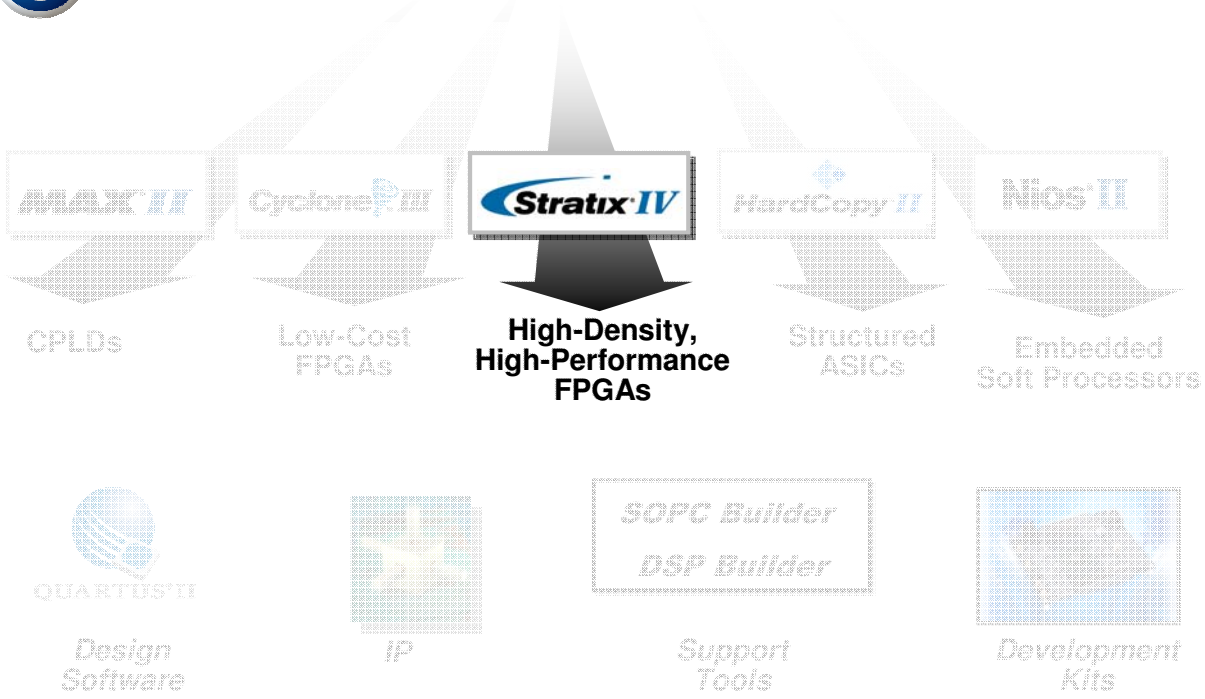

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Introducing Altera 40-nm Solutions

Compromises of the past

Stratix® IV FPGAs
Highest density, highest performance **AND** lowest power

HardCopy® IV ASICs
Benefits of FPGAs **AND** benefits of ASICs

Foundry partnership
Earliest access to 40-nm technology **AND** low-risk path to production

Quartus® II software
Highest performance, highest logic utilization, **AND** fastest compile times

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Stratix IV FPGA: A Closer Look

- Highest density
  - Up to 680K logic elements (LEs)
  - Up to 22.4-Mbits internal RAM
  - Up to 1,360 18 x 18 multipliers
- Highest bandwidth and performance
  - Up to 48 transceivers operating up to 8.5 Gbps
  - Up to 4 x8 hard intellectual property (IP) blocks for PCI Express Gen 1 and Gen 2
  - Up to 748 giga multiply-accumulate operations per second (GMACS) digital signal processing (DSP) performance
  - 2 speed grade performance advantage
- Lowest power
  - Programmable Power Technology
  - Quartus® II PowerPlay technology
  - 40-nm process benefits including 0.9V core voltage
- Seamless FPGA prototyping to HardCopy ASIC production
- Quartus II 8.0: #1 in Performance and Productivity

Highest density, highest performance AND lowest power

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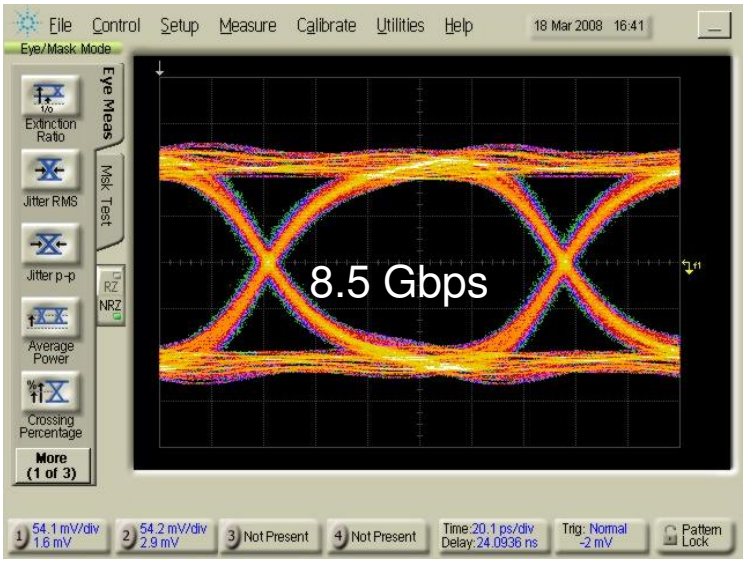
Excelent 40nm Transceiver Test Chip Results

- Transceiver test chip results
  - Pattern: PRBS 7
  - V_{od}: 600 mV
  - DJ: 10.3 ps
  - RJ (RMS): 1.23 ps
- Excellent jitter performance
- Low-risk path to production
- Watch the demo video at www.altera.com/b/40-nm-stratix-iv-video.html



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Protocoll Support

Protocol	HardCopy IV ASICs	Stratix IV FPGAs
3G Protocols		
PCI Express Gen 1 (x1, x2, x4, x8), PCI Express Cable	✓	✓
Serial RapidIO® (1x, 4x)	✓	✓
Gigabit Ethernet, XAUI (IEEE 802.3ae), HiGig+	✓	✓
3G Basic (proprietary), 3G SerialLite II	✓	✓
CPRI v3.0, OBSAI v2.0/RP3-01 v4.0	✓	✓
SONET OC-3/12/48, GPON	✓	✓
SATA, SAS	✓	✓
SD, HD and 3G SDI, ASI	✓	✓
Serial Data Converter (JESD204)	✓	✓
SFI 5.1	Up to 8 Channels	✓
HyperTransport 3.0	Up to 8 Channels	✓
6G Protocols		
PCI Express Gen 2 (x1, x2, x4, x8)	✓	✓
HiGig2, CEI 6G (SR/LR), Interlaken, DDR-XAUI, SPAUI	✓	✓
6G basic (proprietary), 6G SerialLite II	✓	✓
6G CPRI/OBSAI	✓	✓
Fibre Channel (FC1/FC2/FC4)	✓	✓

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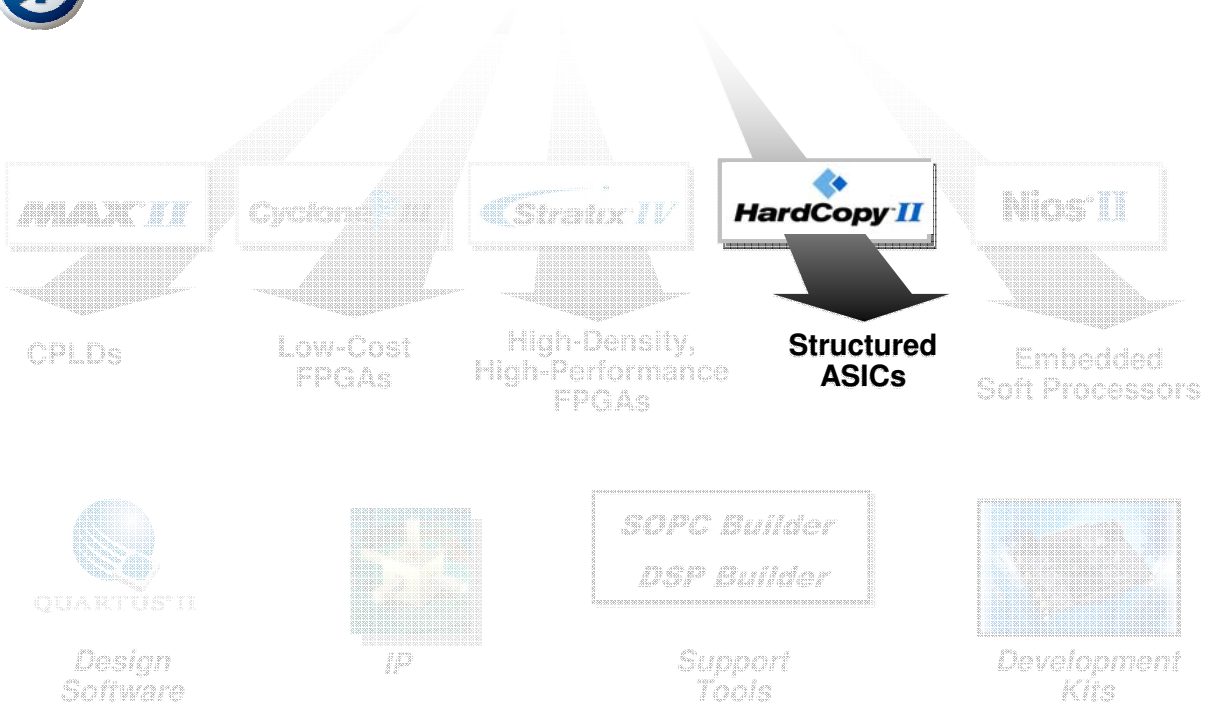

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Hardcopy: A Closer Look

- Seamless prototyping
  - One design, one register transfer level (RTL), one IP set, one tool delivers FPGA and ASIC implementations
- Now with transceivers
- Low risk, lowest total cost access to deep sub-micron ASIC benefits
- Low power
  - 50 percent or lower than companion FPGA
- Guaranteed first-time right

The benefits of FPGAs AND the benefits of ASICs

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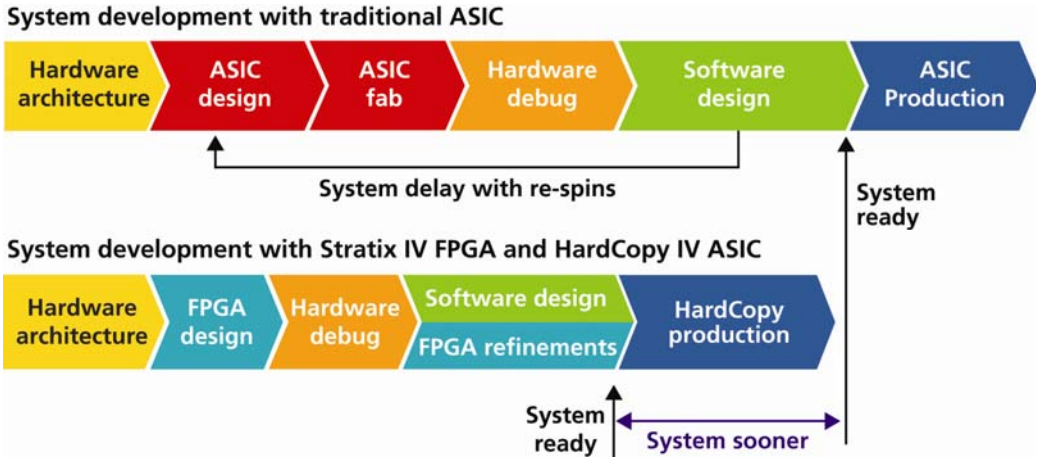
Ultimate System Development Methodology

- Traditional method: Sequential hardware, ASIC, and software development
- Traditional ASIC respins stop everything and delay software completion



- FPGA flexibility speeds system verification and software development
- Saves 9 – 12 months in time to market

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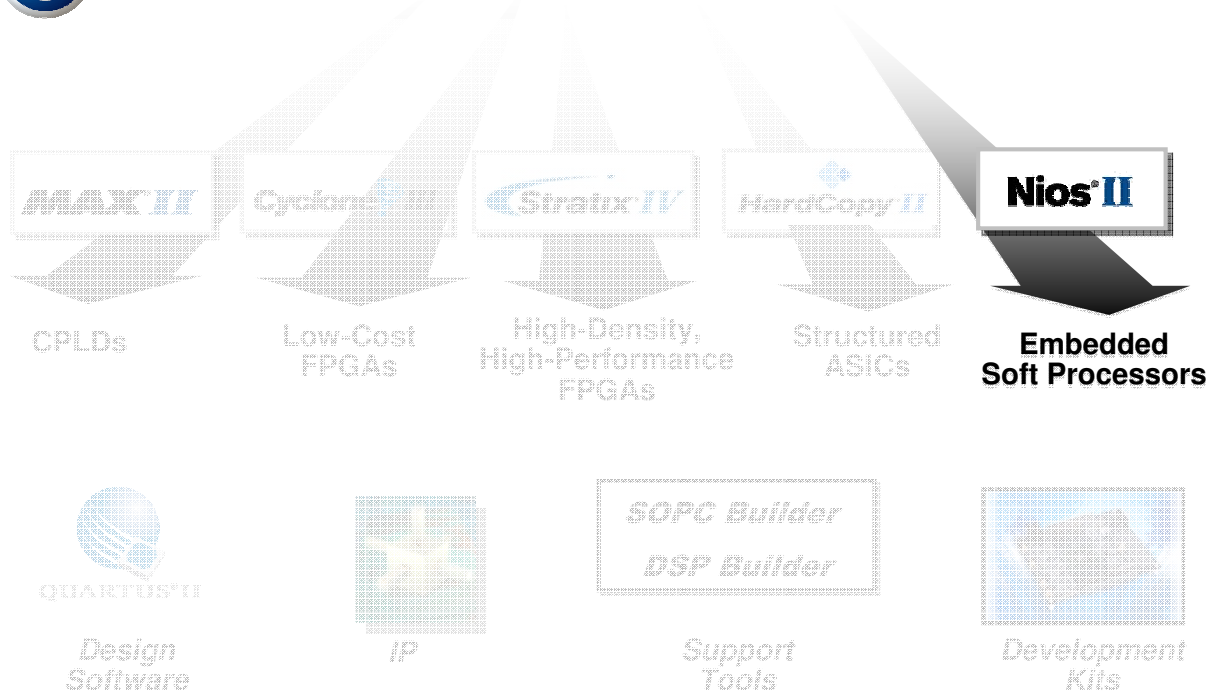
A Complete Solutions Portfolio



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NIOS II – World's most popular Soft Processor

- Over 20,000 development kits shipped
  - Used in communications, consumer, industrial, medical, automotive, and broadcast products worldwide
  - Used by all of the top 20 OEMs
- Active Nios design community (www.niosforum.org)
  - Over 8,000 active members

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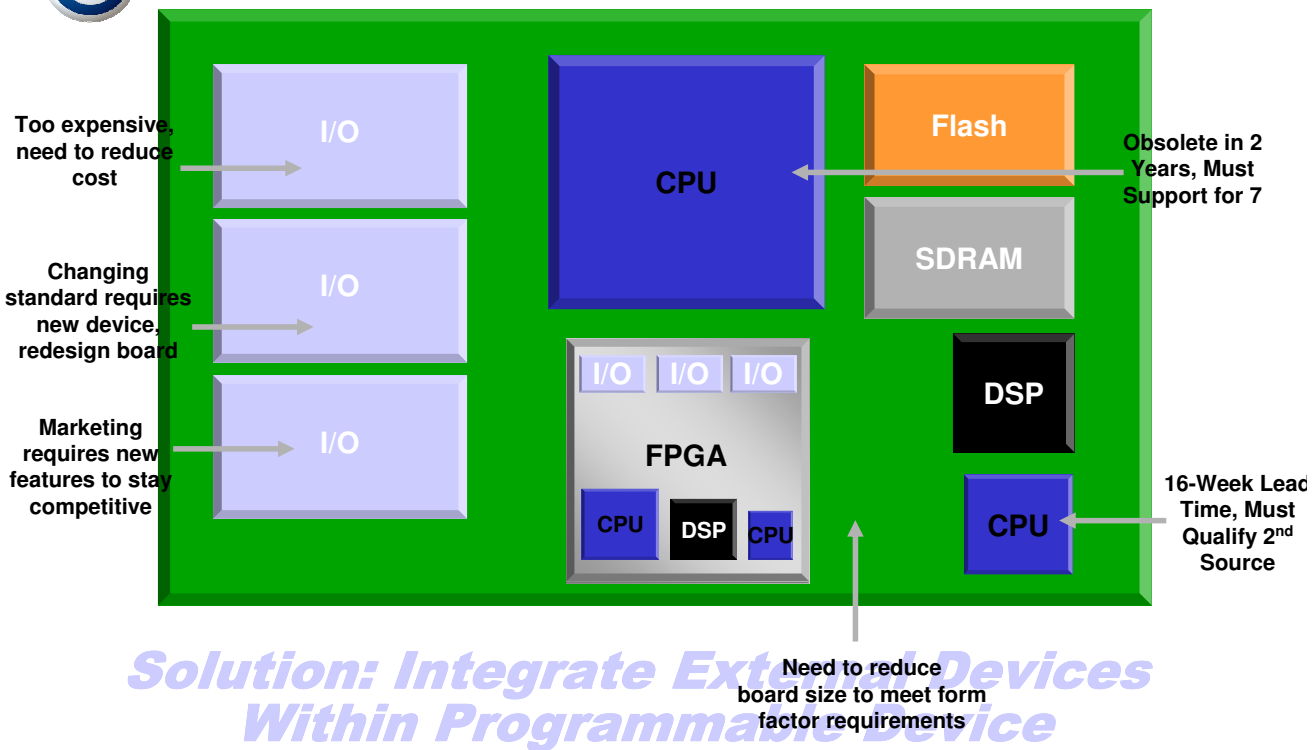
System Design Challenges



Solution: Integrate External Devices Within Programmable Device

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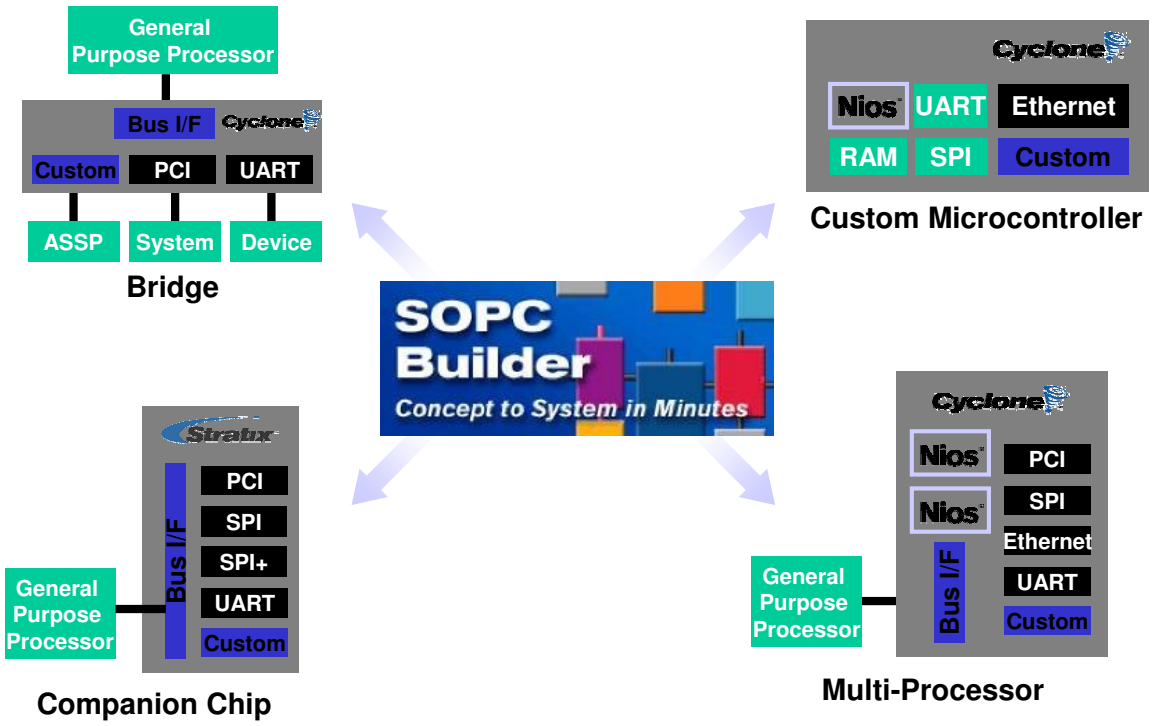
SOPC Builder – System Generation Tool



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Motion Control in FPGA

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FalconEye-FPGA

- **400V BDC Motion Control Development Kit**
- Contains of :
  - FalconEye – Power Board
  - Mercury Code – DBC3C40
  - BISS Encoder
  - BDC Motor
  - VHDL Modules
  - C- Files as a reference to demonstrate the System
- Developed by FH-Cologne
- Sponsored by Altera, EBV Elektronik

It's not a product!!

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Motion Control based on FPGA?

- **Reduce Number of components**
  - SD ADC Demodulator
  - Digital Encoder Interface
  - Fieldbus IP-Core
  - Soft-CPU NIOS II
- **Increase Performance**
  - No Sampling Issues
  - No Calculation Delay
  - High switching frequency
- **Increase Flexibility**
  - Platform strategy
  - Scalability
  - Less Option Cards

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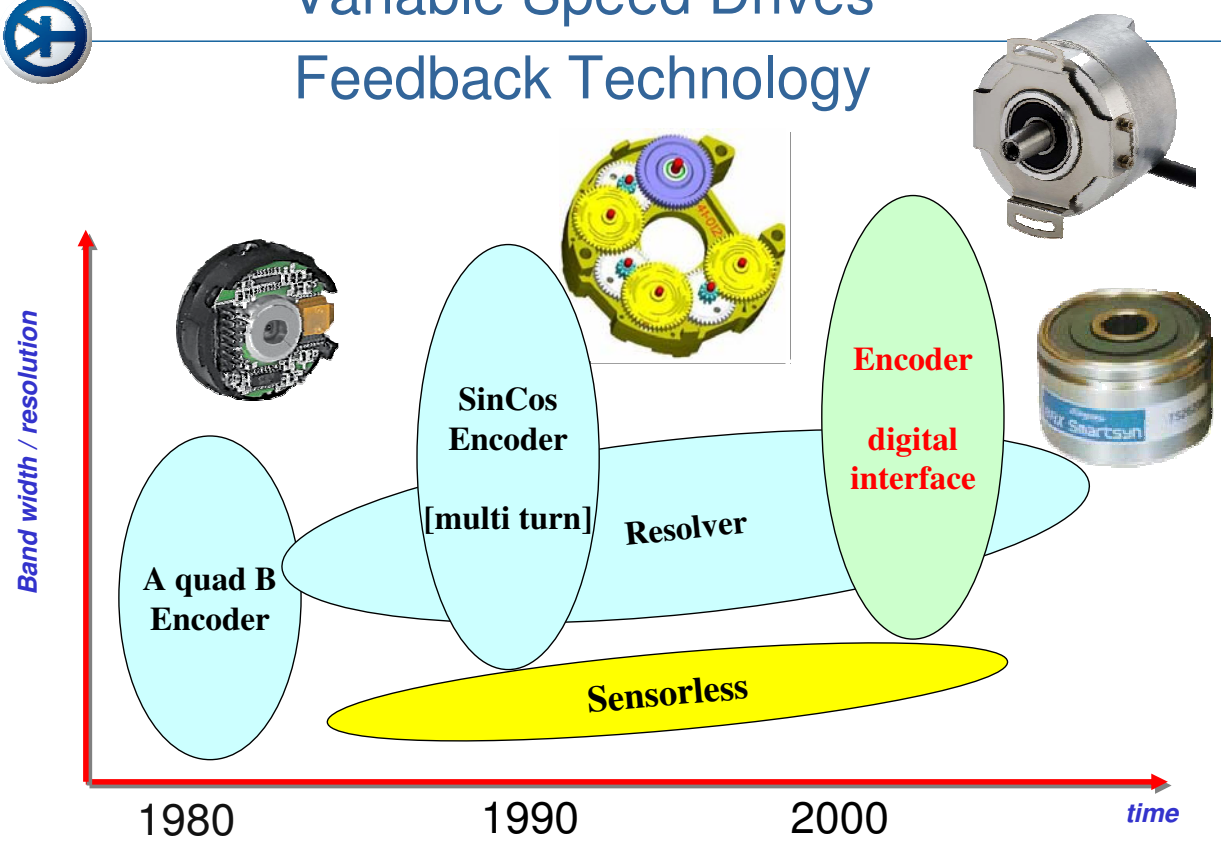
Variable Speed Drives
Feedback Technology



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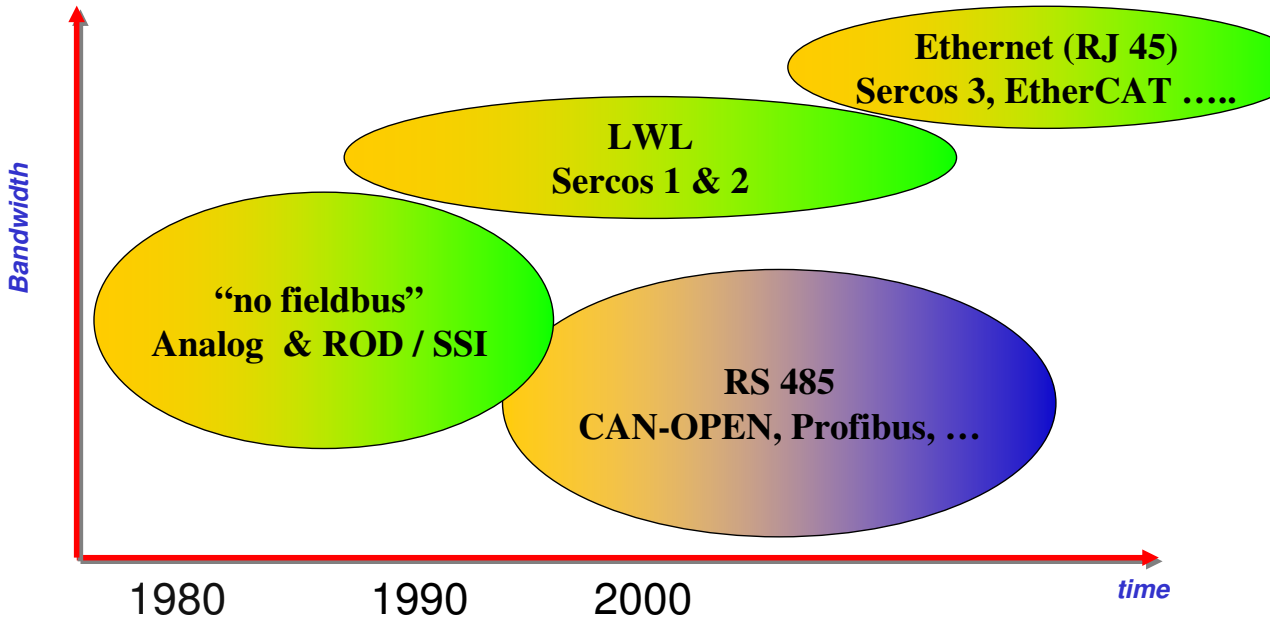
Motion Fieldbus - Technology



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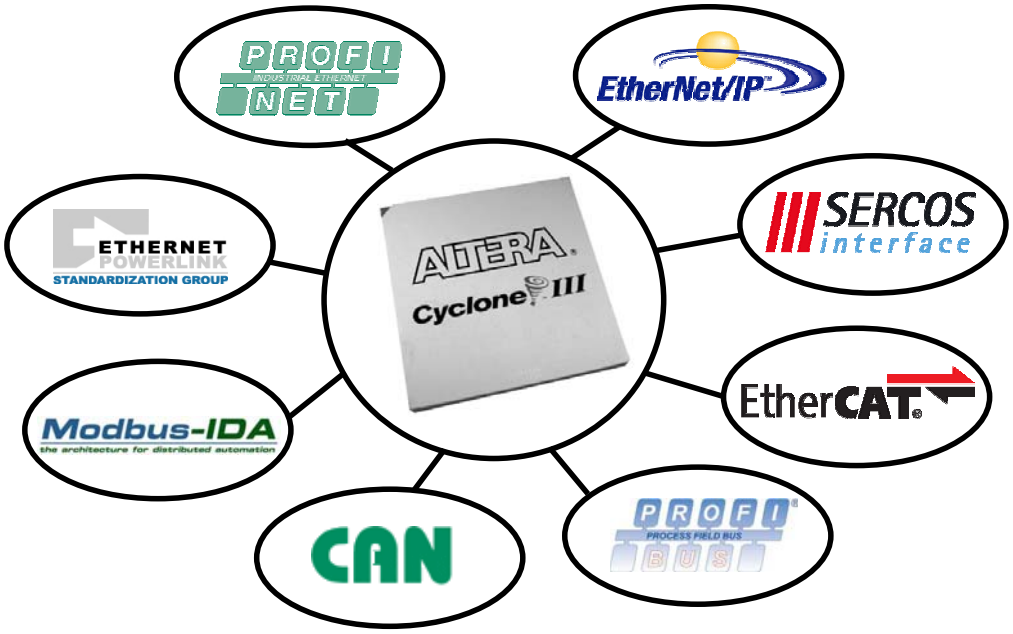
Industrial Communication



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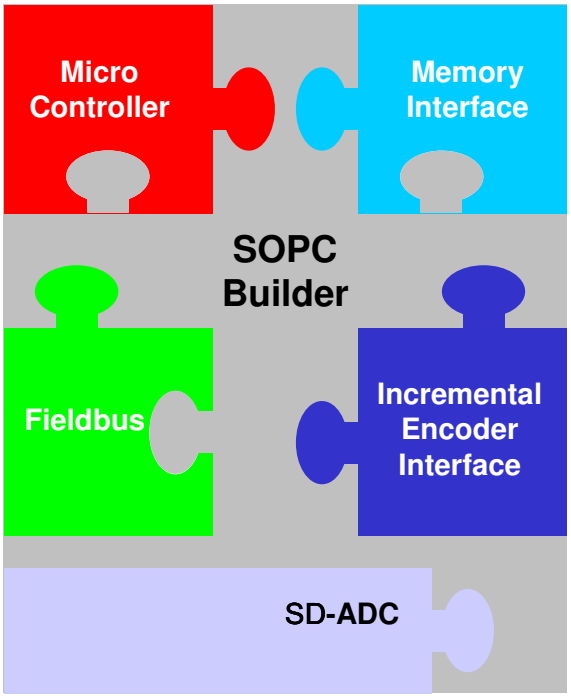
IP Core – Integration

- Automated Integration Tool
- GUI - Based
- Build bridges between IP-Cores
- Automatically resolves :
  - Clock domains
  - Bit widths
  - Arbitration
  - Etc...



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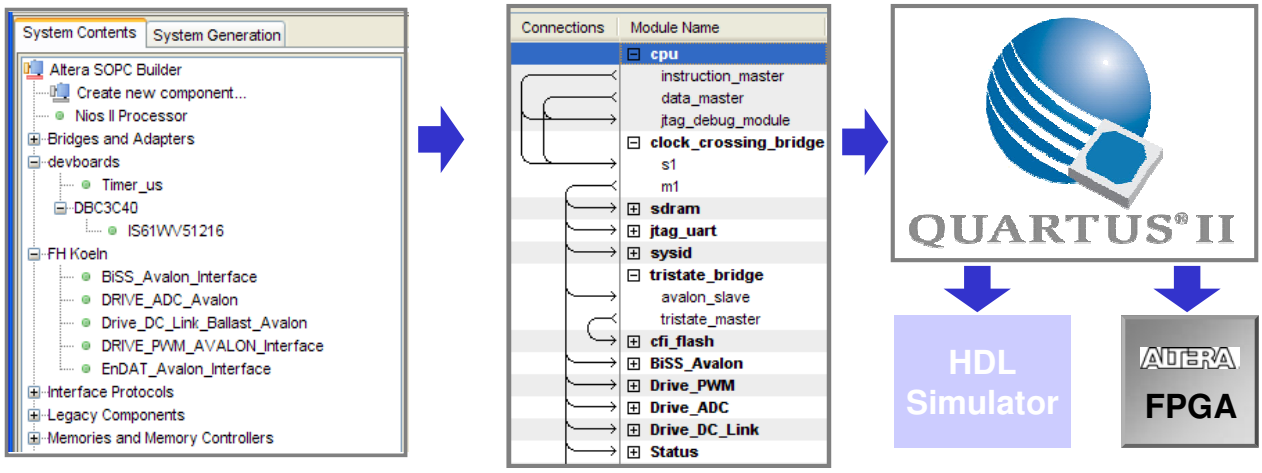
SOPC-Builder System Design

1 Select IP → **2 Select Connections** → **3 Generate System**



Cuts *Weeks* Off Development Time!

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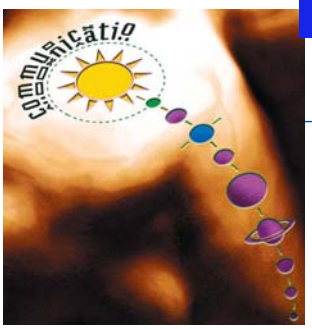
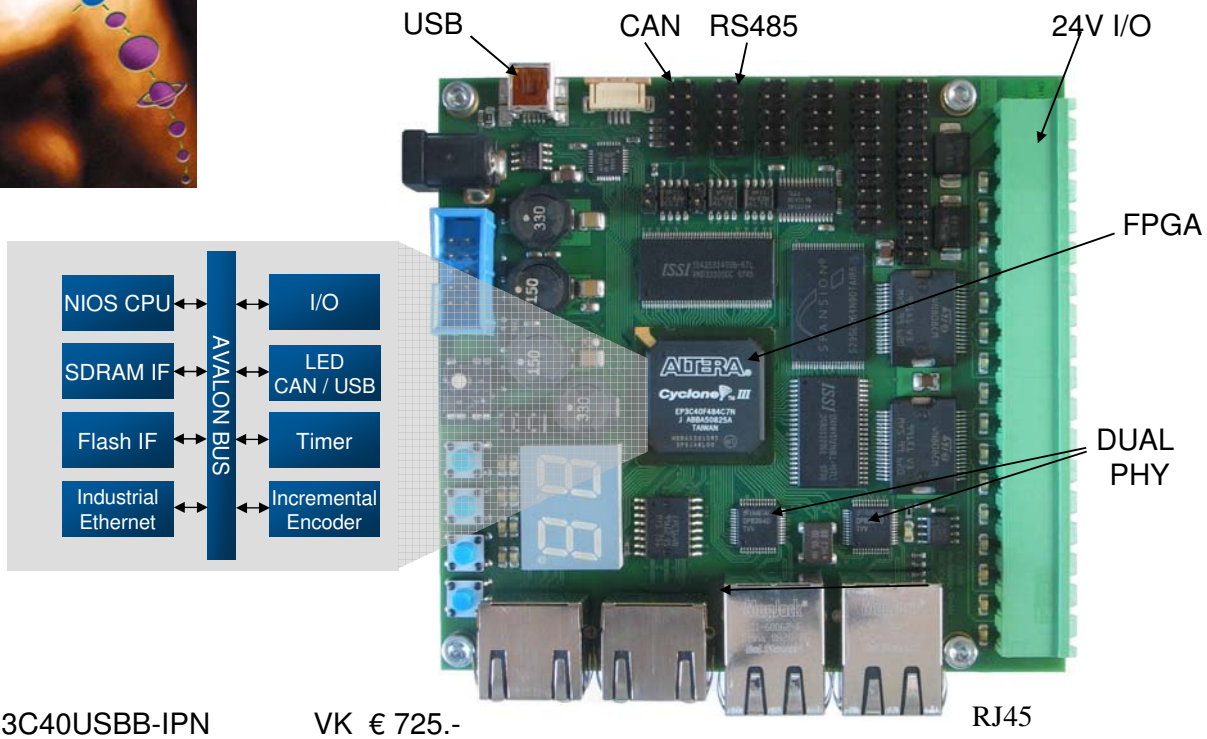


EBV MercuryCode Board



- DBC3C40USBB-IPN VK € 725.-

(full NIOSII-license + USB-Blaster included)

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Nios goes .Net

- IEC61131 (SPS-programming) Language and c# support for NIOS
- eCLR for Microsoft Intermediate Language
- Microsoft Express Studio
- First Embedded Implementation (NIOSII)
- More information @ www.kw-software.de
- Evaluation version included in every DBC3C40 Kit

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Codesys Solution available on NIOS II

- 3S-Smart Software Solutions is the manufacturer of the market leading IEC 61131-3 programming tool CoDeSys.
- Starter package of the CoDeSys 3.0 run time system available for Nios II
- The implementation for the NIOS II Core also includes hardware functions like E/As, field bus interfaces or Ethernet ports.
- Evaluation version available for DBC2C20 EVAL-Board
- More Information @ http://www.3s-software.com

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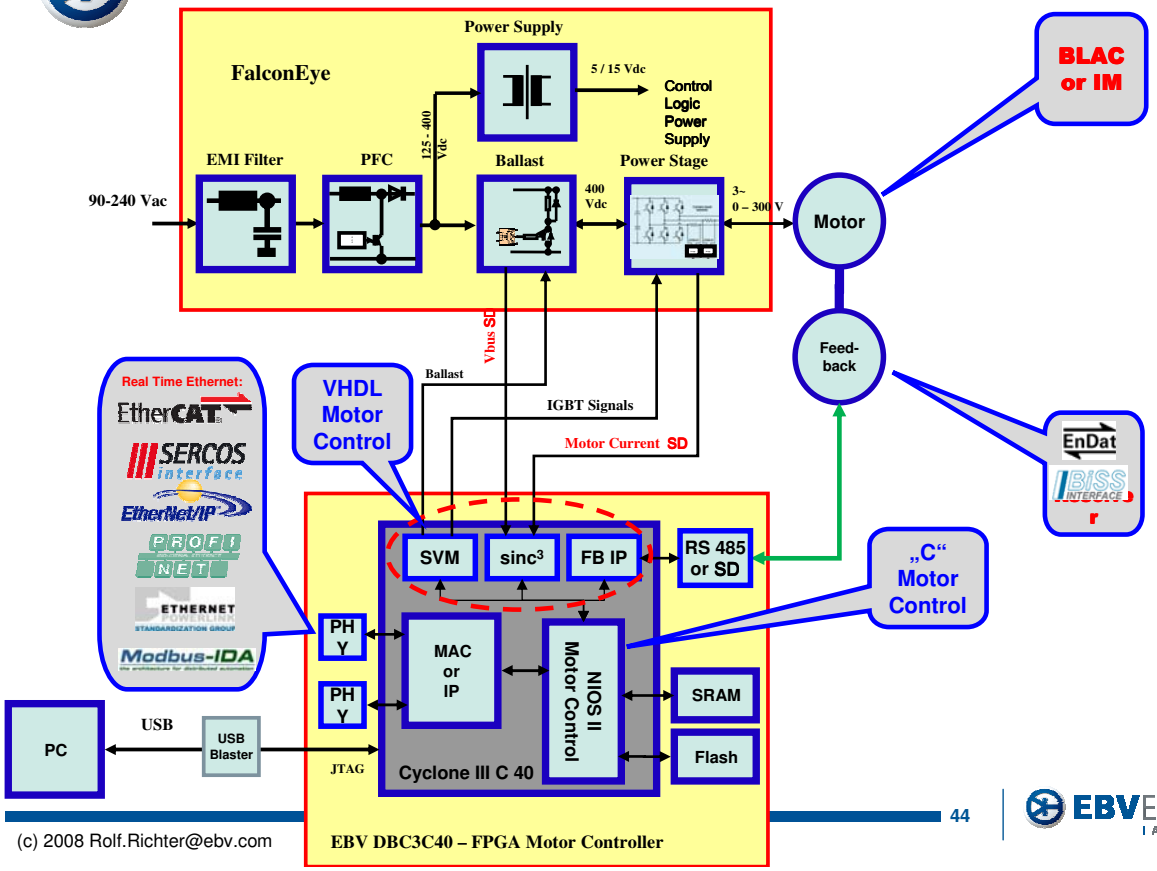
FalconEye-FPGA based Motor Control



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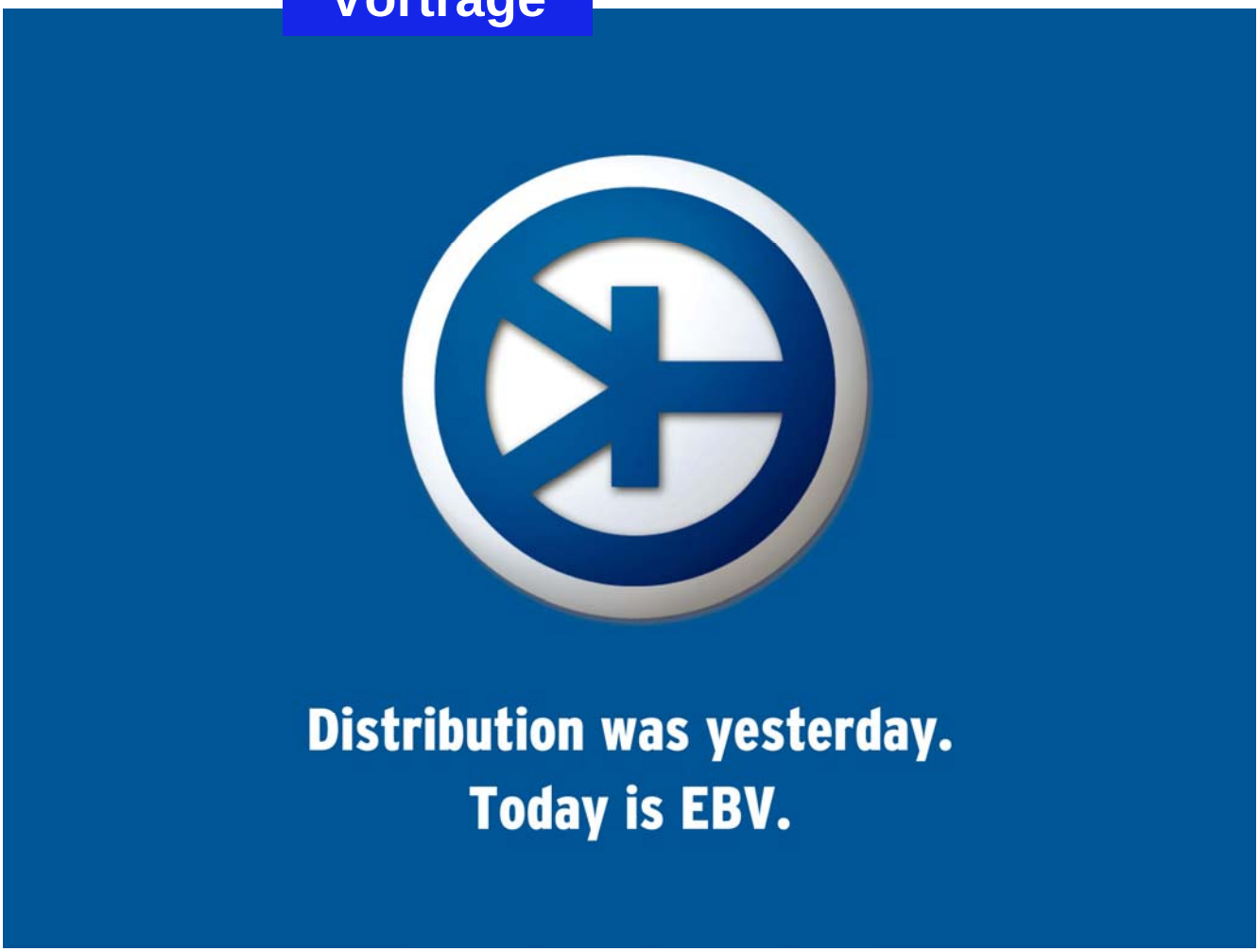
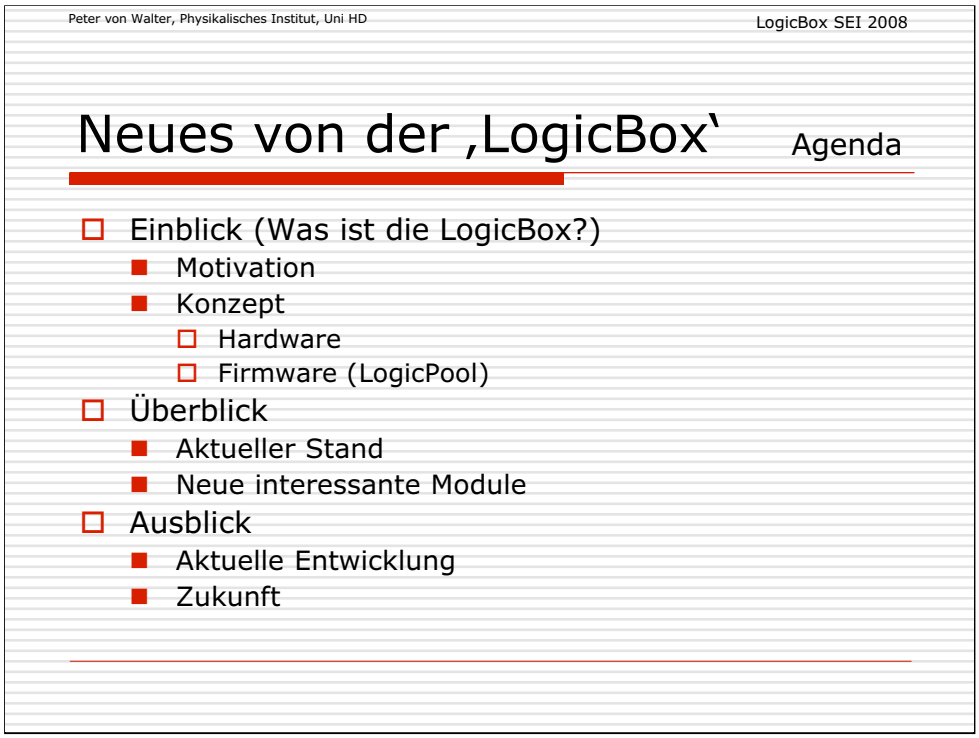
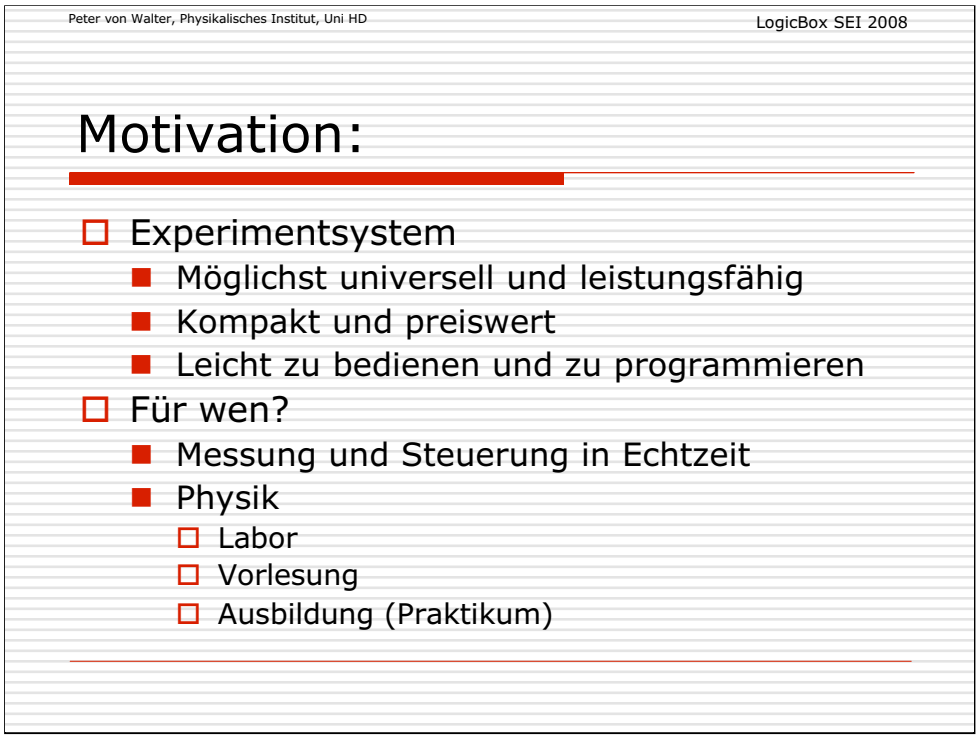

Distribution was yesterday.
Today is EBV.



Was hat sich seit der Einführung der „LogicBox“ auf der SEI Herbsttagung 2006 in Heidelberg getan?

Es wird nocheinmal kurz das Konzept und der aktuelle Stand sowie interessante neue Funktionsmodule vorgestellt.



Warum und für wen wurde das System entwickelt?

Vor allem in den Bereichen Physik wird die LogicBox bereits vorteilhaft eingesetzt und ist mittlerweile auch kommerziell durch die Fa. WIENER erhältlich.

LogicBox: Hardware

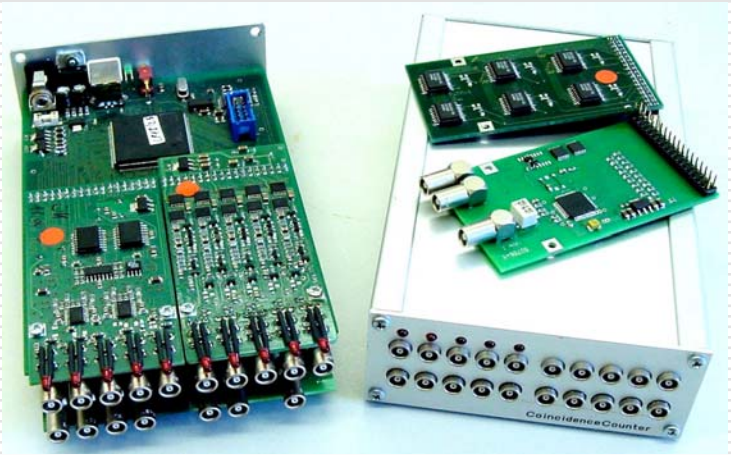
- DL7xx: FPGA-Box
  - Interface: Parallel, USB, VME
  - Zentrale Logik: FPGA
- SU7xx: austauschbare Submodule (1...4)
  - Digital I/O: TTL, TTL^{coax}, NIM, LVDS, ...
  - Analog I/O: Discriminator, ADC, DAC, ...
  - Anzeige: LEDs
  - Intern: Memory, Delay...
  - Anwenderspezifisch: QDA, IF, ...

Die Hardware setzt sich aus zwei Einheiten zusammen:

-Einer universellen FPGA-Basiskarte mit USB-Interface

-Den anwendungsspezifischen Subkarten für den digitalen und analogen I/O

DL701: FPGA Box



Das Bild zeigt zwei mit jeweils 4 Subkarten voll bestückte Geräte.

LogicBox: FPGA-Boards

Typ	Aufbau	IF	FPGA	Sonstiges
DL701	3HE/4 SU	USB 1.1	XC3S400	
DL702	6HE/4 SU	VME	Altera	nicht kompatibel
DL703	3HE/4 SU	Parallel	XC3S400	
DL704	3HE/4 SU	Parallel	-	
DL705	3HE/4 SU	USB 2.0	XC3S400	
DL706	NIM/4 SU	USB 2.0	XC3S400	
DL707	3HE/4 SU	USB 2.0	XC3S4000	
DL708	NIM/4 SU	USB 1.1	XC3S400	
DL709	NIM/8 SU	USB 2.0	XC3S4000	In Planung!
DL710	6HE/4 SU	VME	XC3S4000	

USB 2.0:
- Firmware via USB ladbar.
- LogicPool Setup für Powerup speicherbar.

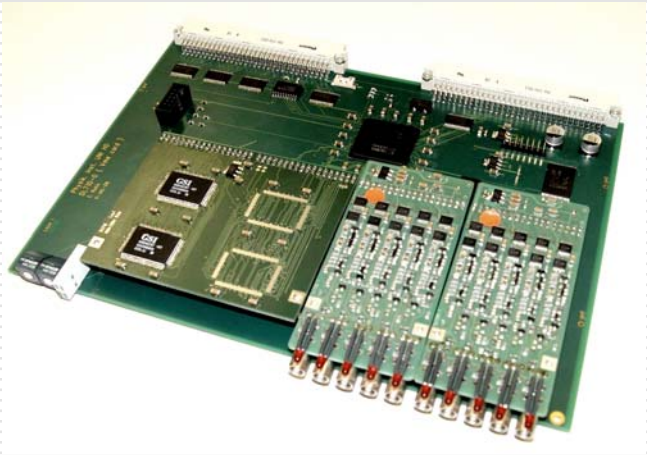
Mittlerweile gibt es eine Reihe von Basiskarten in verschiedenen Bauformen, Interfaces und FPGA-Größen.

Die Subkarten können auf allen Basiskarten in der gleichen Weise eingesetzt werden.

Bei den Geräten mit USB 2.0-Interface ist die Firmware auch über USB nachladbar sowie der Setup für die Verschaltung der LogicPool-Module im Gerät selber speicherbar.

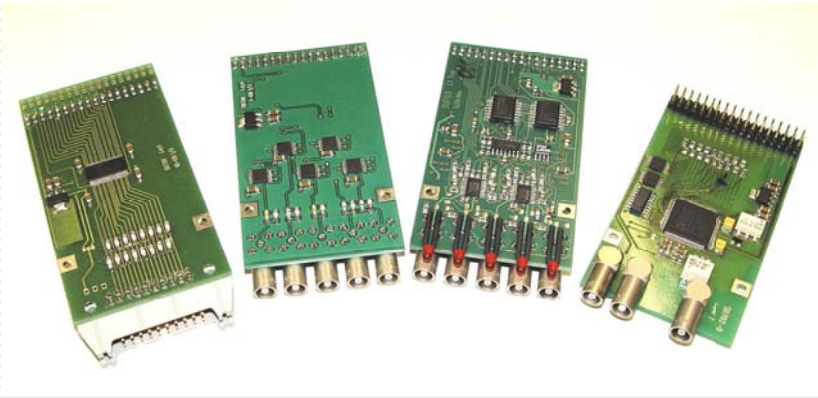
Als Beispiel der Aufbau einer LogicBox als NIM-Modul und mit 4 Subkarten.

DL710: VME



Hier ist eine VME-Karte mit großem FPGA (XC3S4000), einem teilweise bestücktem Memory-Modul und zwei NIM/TTL-IO Karten mit Leuchtdioden zu sehen.

SU7xx: Submodules



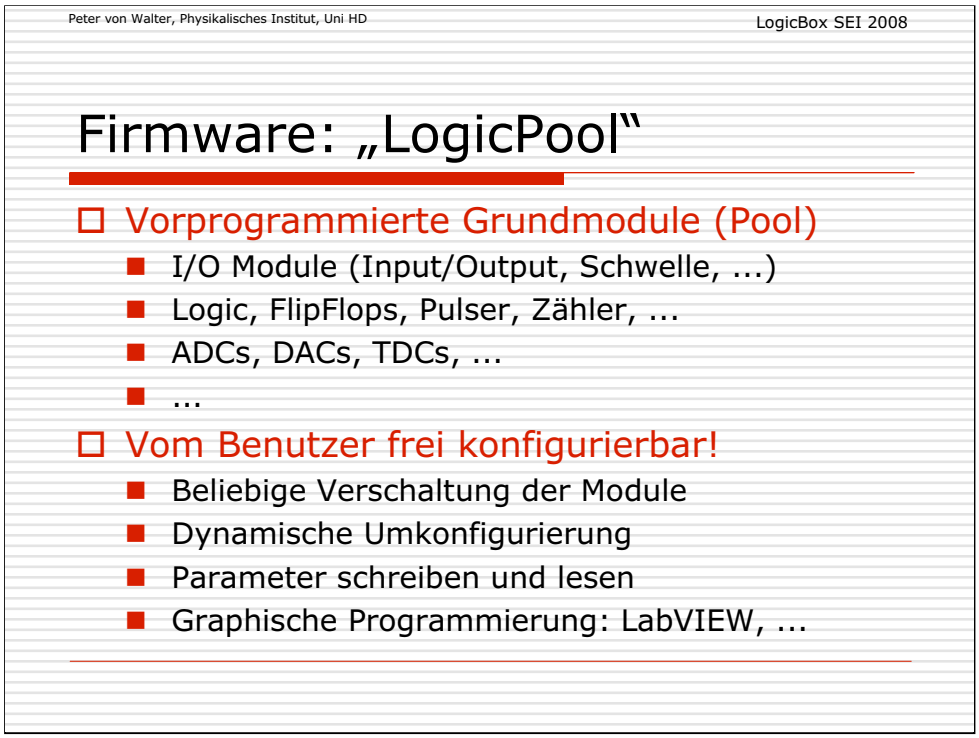
Eine Auswahl von verschiedenen Subkarten.

LogicBox: Sub-Boards

Typ	Beschreibung
SU700	5x TTL I/O – LEMO coax
SU701	16x TTL I/O - Multiconnector
SU702	8x ADC, Diff, bipolar
SU703	4x Discriminator and 1x TTL I/O –coax, std
SU704	5x NIM/TTL I/O – LEMO coax
SU705	16 MByte RAM (100 MHz statisch)
SU706	1x ADC (100 Mhz) ,2x TTL I/O – LEMO coax
SU707	8 x LVDS I/O
SU708	Cascade IF50 Interface
SU709	8 x Temperaturesensor
SU710	2x Fast DAC (100 Mhz)
SU711	6 x programmable Delayline 0,5ns .. 128 ns
SU712	16 x ADC (5 us, 14 Bit)
SU713	16 x DAC (14 Bit)
SU714	HAL25 Interface
SU715	NF-Amplifier with prog. Gain
SU716	16 M * 32 Bit RAM (100 MHz statisch)
SU717	QDC, Ladungsempfindlicher ADC

Es sind mittlerweile Subkarten für fast alle digitalen und analogen IO-Standards verfügbar.

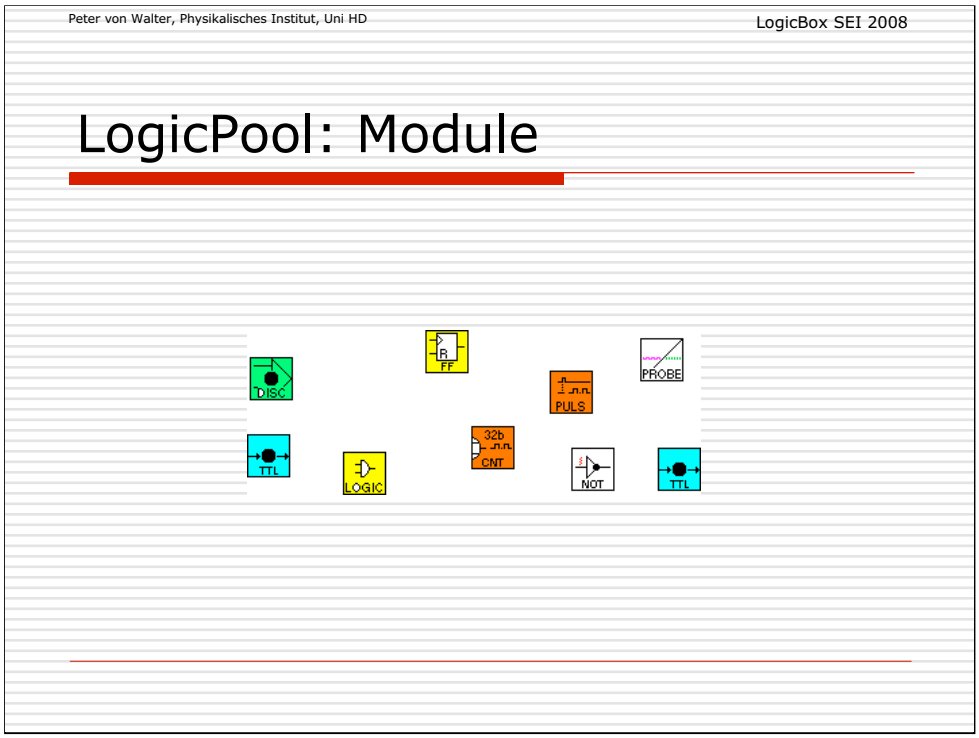
Einige Karten wurden speziell für bestimmte Anwendungen und Experimente entwickelt.



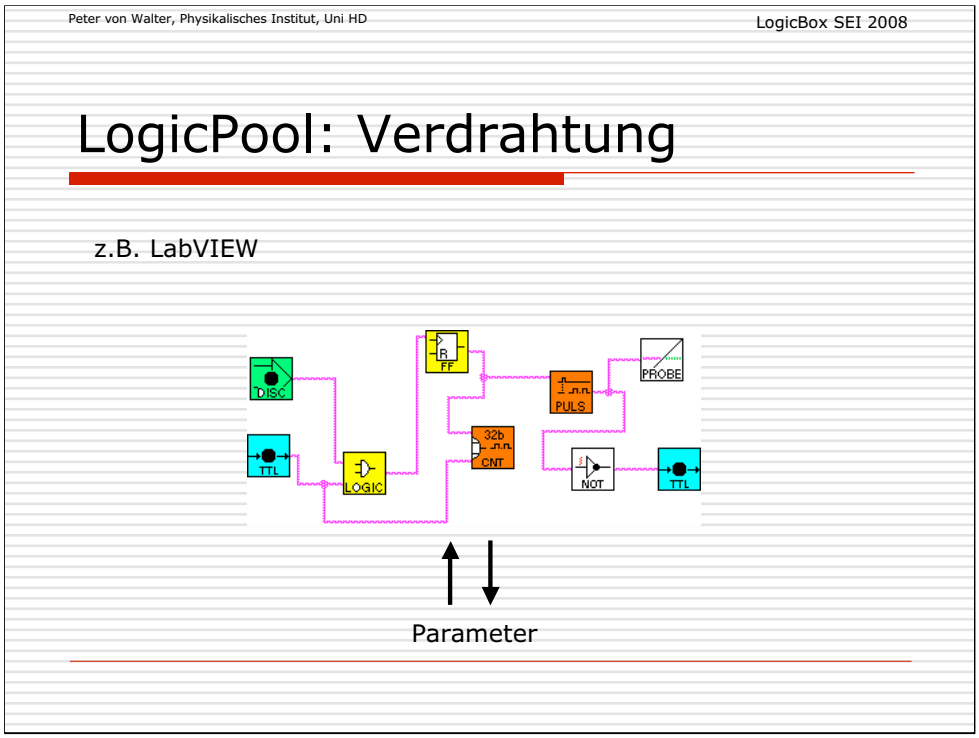
Um die Programmierung von gewünschten Funktionen sehr leicht durchführen zu können wurde das Konzept des „LogicPools“ entwickelt:

Typische Grundfunktionen sind bereits im FPGA implementiert und können für die Gesamtfunktion frei verschaltet werden.

Dabei ist eine Vielzahl von Parametern setzbar oder auslesbar.



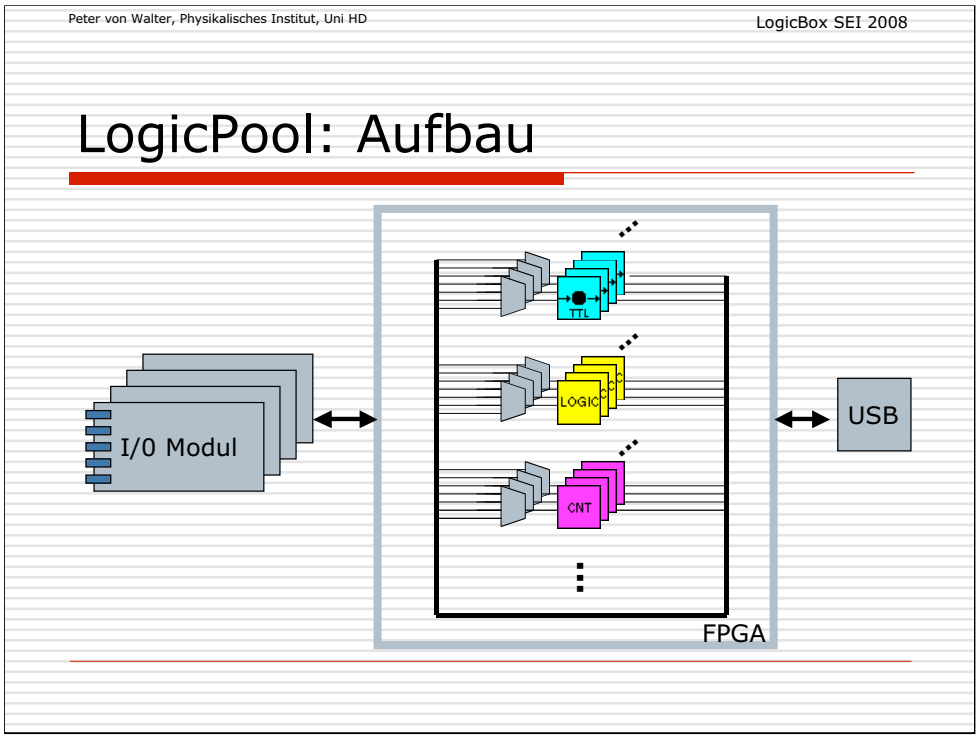
Vorgefertigte Funktionsmodule dienen als Signal-IO sowie zur digitalen Verarbeitung, wie z.B. Logic, Zähler, usw. !



Die frei programmierbare Verdrahtung der Funktionsmodule erlaubt eine beliebige Verschaltung.

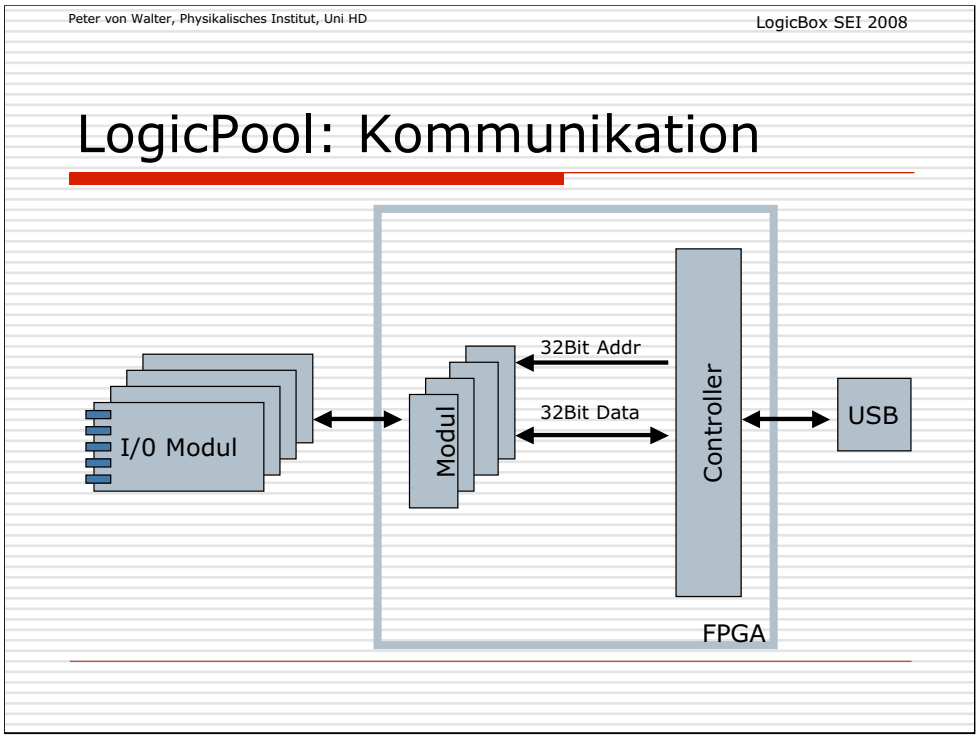
Zusätzliche Parameter (z.B. Zählerstand) können gesetzt oder ausgelesen werden.

LabVIEW erlaubt wie in einem Schaltbild die Schaltung zu zeichnen und übernimmt die Programmierung.



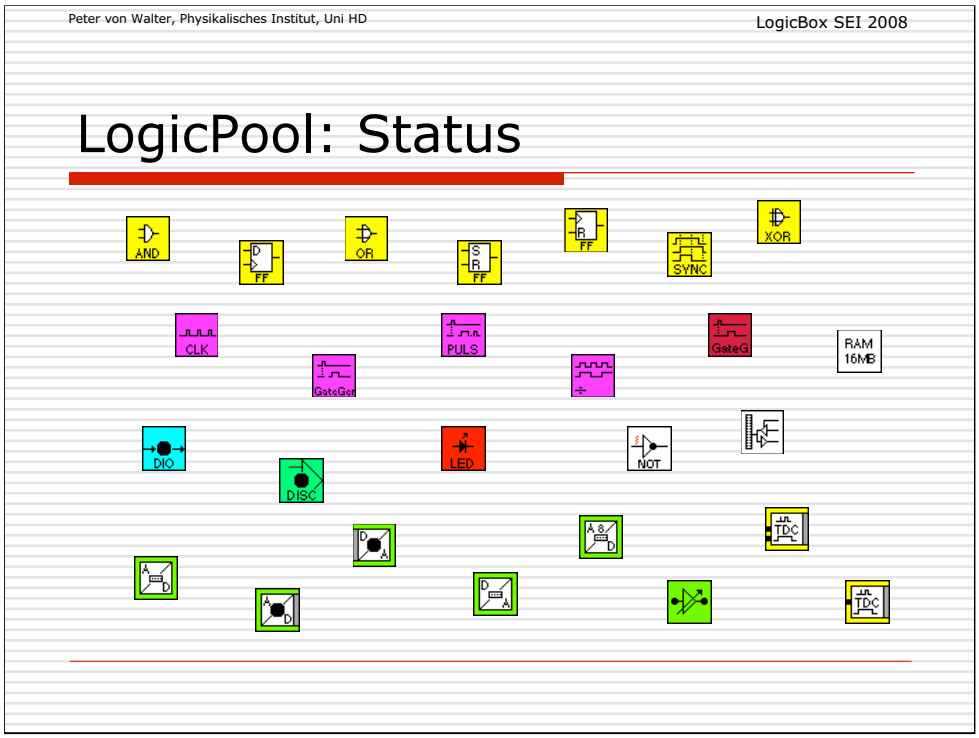
Alle Funktionsmodule im FPGA besitzen Ausgänge, die über Multiplexer an den Eingängen ausgwählt werden können und damit jede beliebige Verschaltung der Module ermöglichen.

Bestimmte Module sind mit den Subkarten verbunden und realisieren den Signal-IO oder bestimmte Hardwarefunktionen.

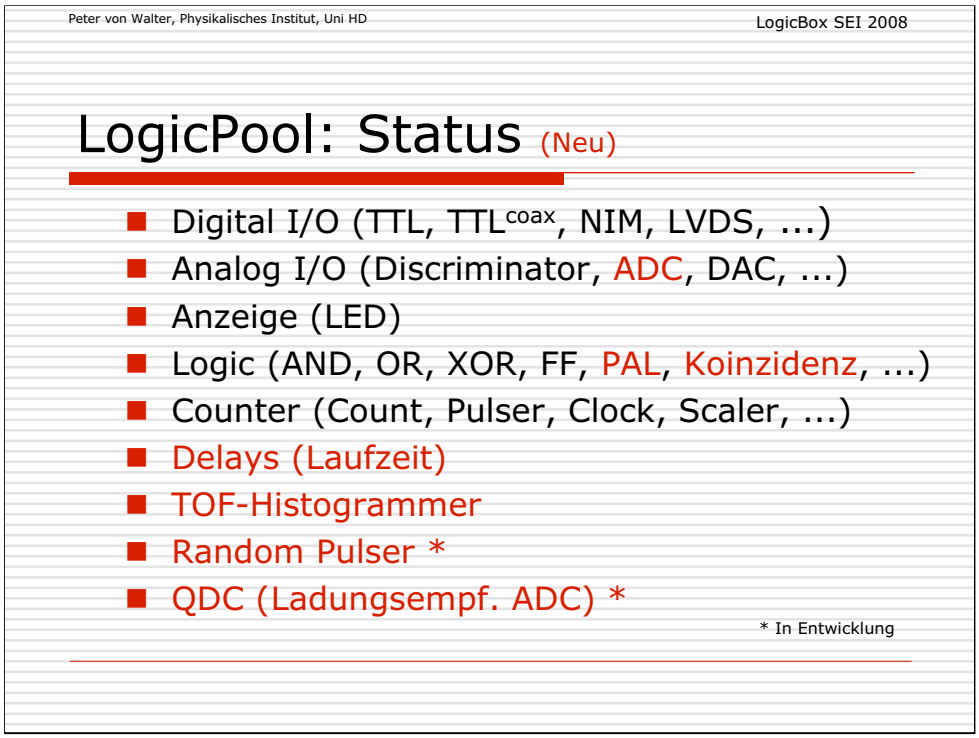


Die interne Kommunikation ist über einen 32 Bit Address- und Datenweg möglich.

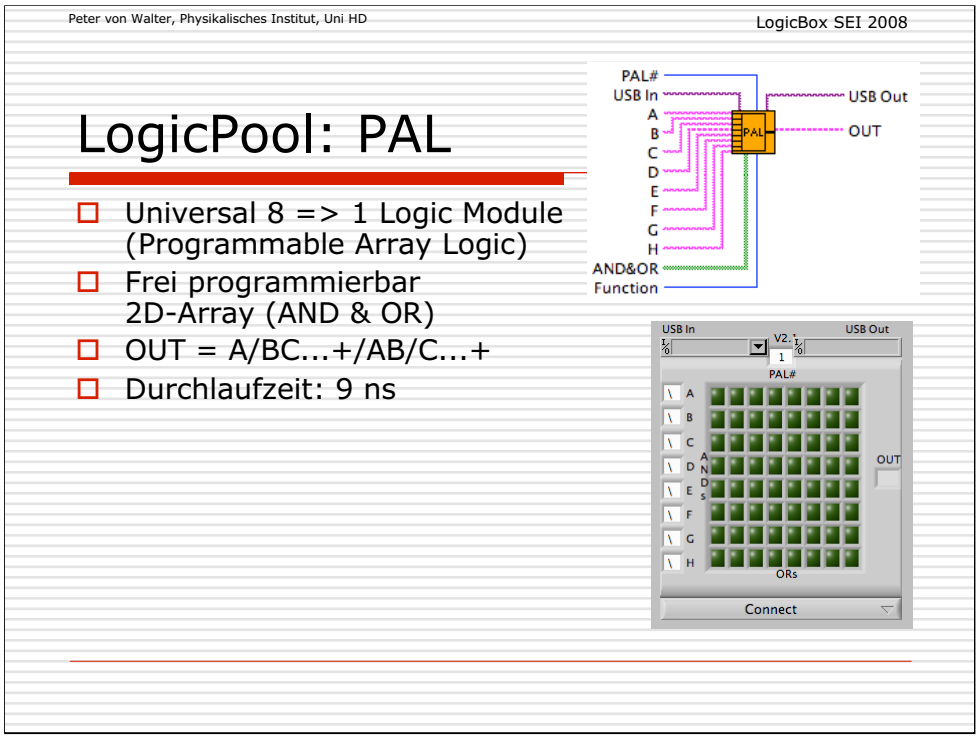
Ein Controller übernimmt die Umsetzung des USB-Protokolls auf den internen Datenweg.



Der aktuelle Status ist gekennzeichnet durch eine Vielzahl von Funktionsmodulen, die eine breite Basis von Anwendungen abdecken soll!



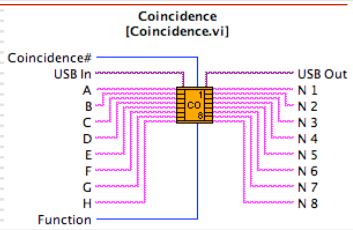
Neuere Module (rot) kommen aus speziellen Anforderungen und sind für hohe zeitliche und funtionelle Verarbeitung entwickelt.



Um logische Funktionen hoher Funktionstiefe von mehreren Eingängen auf einen Ausgang zu realisieren, wurde dieses Modul entwickelt.

Die logische Funktion wird durch eine programmierbare AND/OR-Matrix (Normalform) bestimmt!

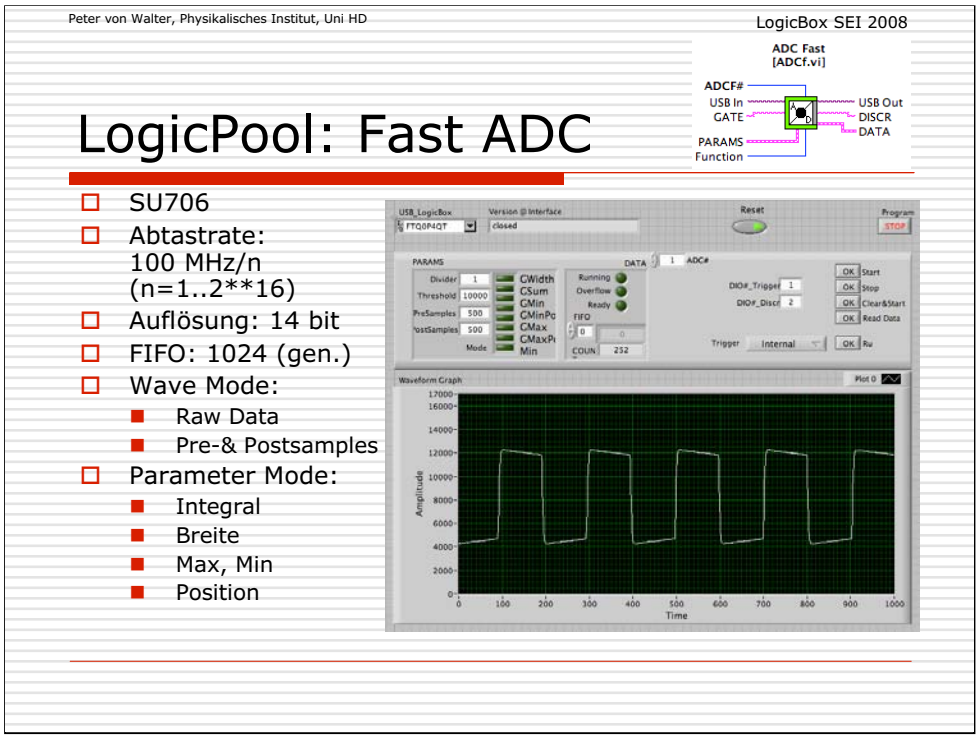
LogicPool: Koinzidenz




```
Coinzidence: process(In_TIG)
   variable KTerm: integer;
begin
   KTerm := 0;
   for i in 1 to Ins loop
      if In_TIG(i)='1' then KTerm := KTerm +1; end if;
   end loop;
   for i in 1 to Ins loop
      if i=KTerm then Outp_TIG(i) <= '1'; else Outp_TIG(i) <= '0'; end if;
   end loop;
end process;
```

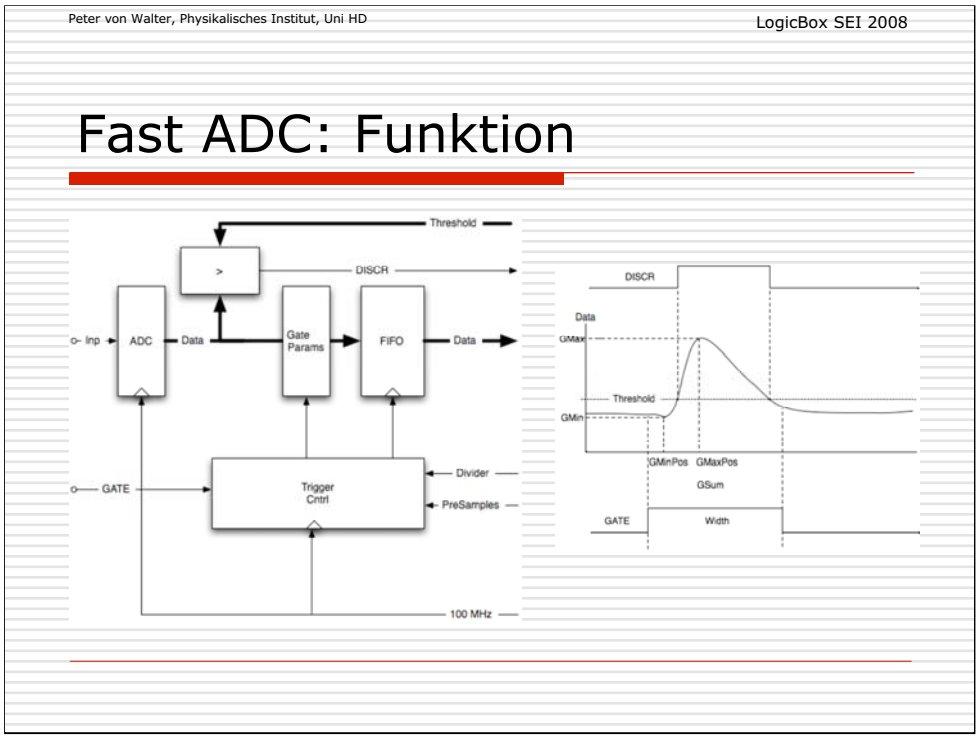
In vielen kernphysikalischen Experimenten muss als Trigger die Koinzidenz (Multiplizität) von mehreren Detektorsignalen bestimmt werden!

Dieses Beispiel zeigt auch, wie einfach eine Beschreibung in VHDL in parametrisierten Form erfolgen kann.



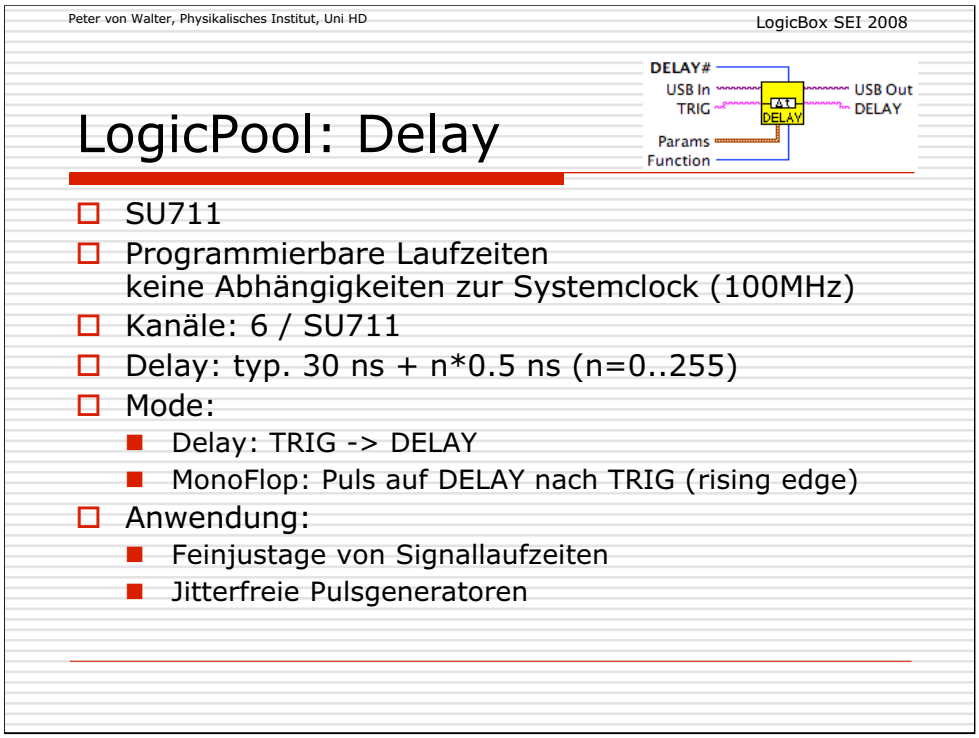
Ein bereits existierendes Modul für einen schnellen (100 MHz) ADC wurde überarbeitet und an Anforderungen mit erhöhter Pulsrate angepasst.

Neben den Rohdaten werden alternativ ausgewählte Puls-Parameter bereits durch die Hardware ermittelt und nur diese in ein FIFO geschrieben. Somit können Totzeiten durch das Auslesen der Rohdaten vermieden werden.

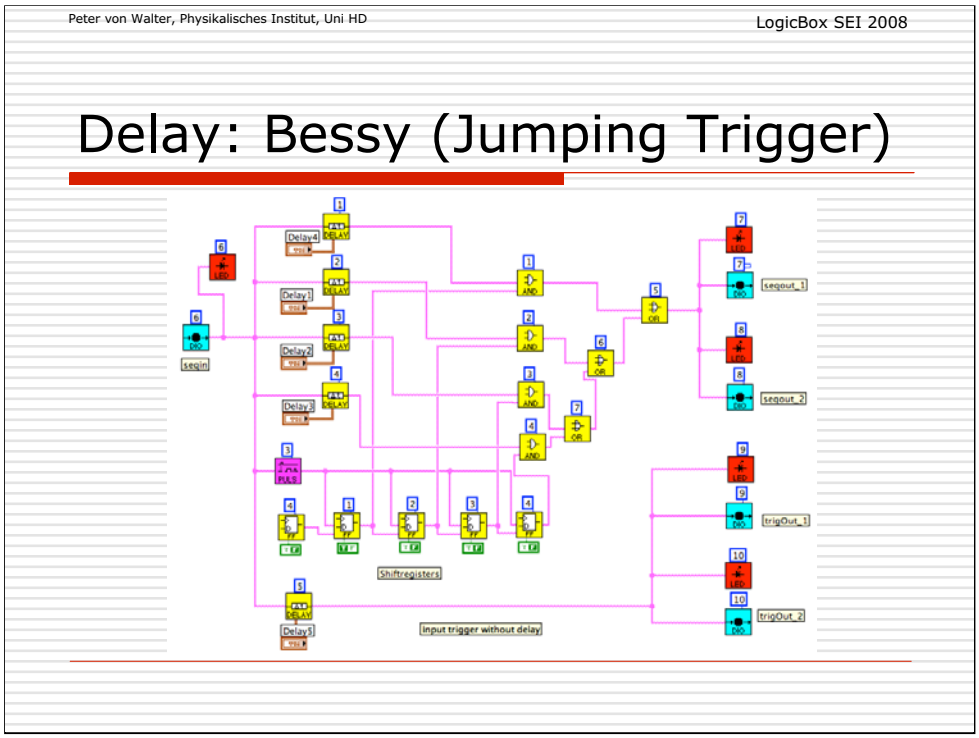


Der **ADC** Baustein sampelt und konvertiert kontinuierlich den analogen Eingang **Inp** mit der Systemclock von **100 MHz**. Die 14 Bit Daten **Data** werden dabei in einem Vergleicher (**>**) mit der **Threshold** verglichen und daraus ein Ausgangssignal **DISCR** abgeleitet.

Der Dual-Port Speicherbaustein **FIFO** speichert die Daten entweder direkt oder nur die entsprechenden Signalparameter, die in der Einheit **GateParams** ermittelt werden. Das Einschreiben der Daten kann abhängig von einem **Divider** entsprechend auch mit einer 100 MHz/Divider langsameren Frequenz erfolgen und so langsamere Abtastraten realisiert werden.

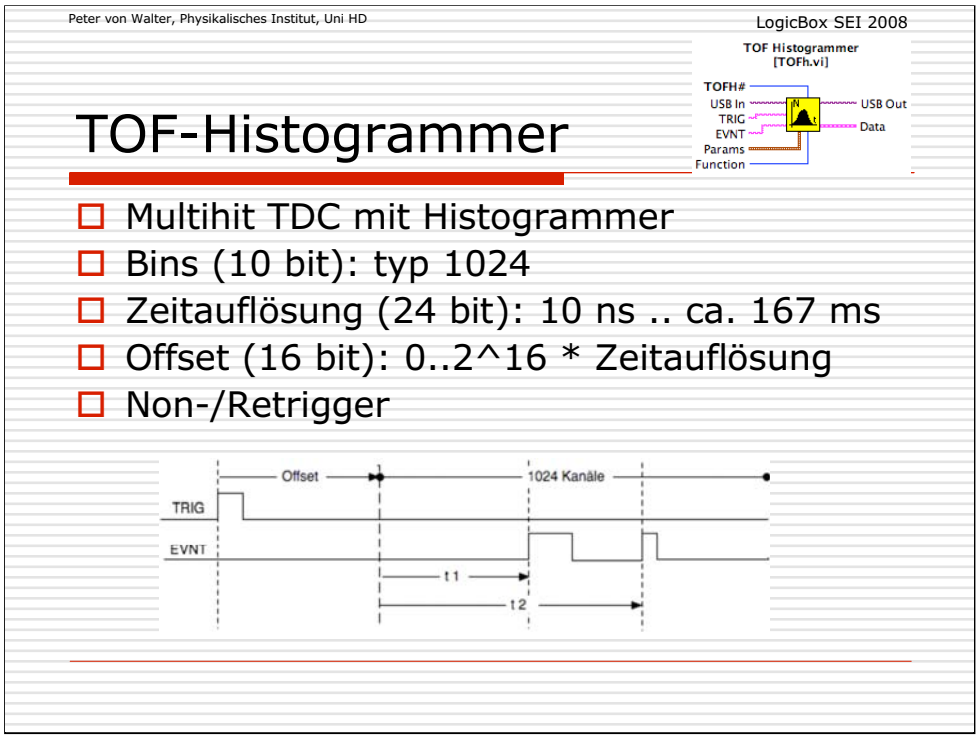


Dieses Modul realisiert in Verbindung mit einem programmierbaren Delay-Baustein (Laufzeit) jitterfreie Verzögerungen.



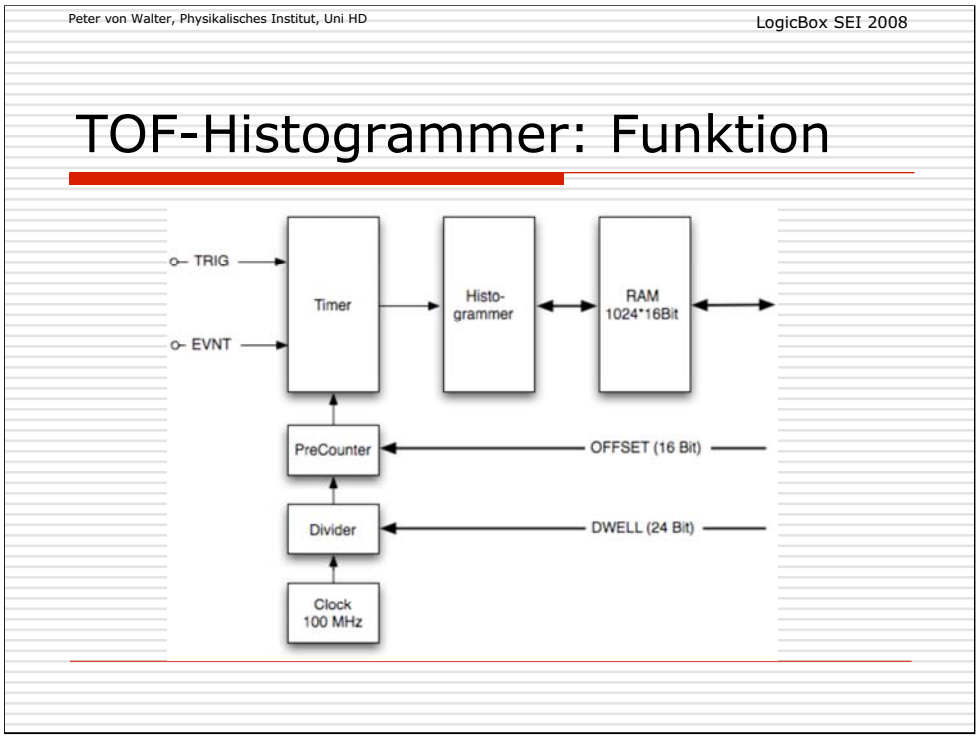
Bei Bessy (Berlin) wurde mit dieser Schaltung ein Trigger für einen Femto-Laser mit alternierender Verzögerung (Jumping Trigger) realisiert.

Die Verzögerung beträgt jeweils 12ns in 4 Stufen mit einer Rate von ca. 3 kHz.



Ein einfacher Zeitmesser (Time Of Flight) für mehrere Events wurde mit einem Zähler (24 Bit bei 100 MHz) aufgebaut.

Die Zeitinformation wird unmittelbar in einem Speicher zu einer Häufigkeitsverteilung (Histogramm) einsortiert. Diese kann unabhängig ausgelesen werden, so daß keine Totzeiten auftreten.

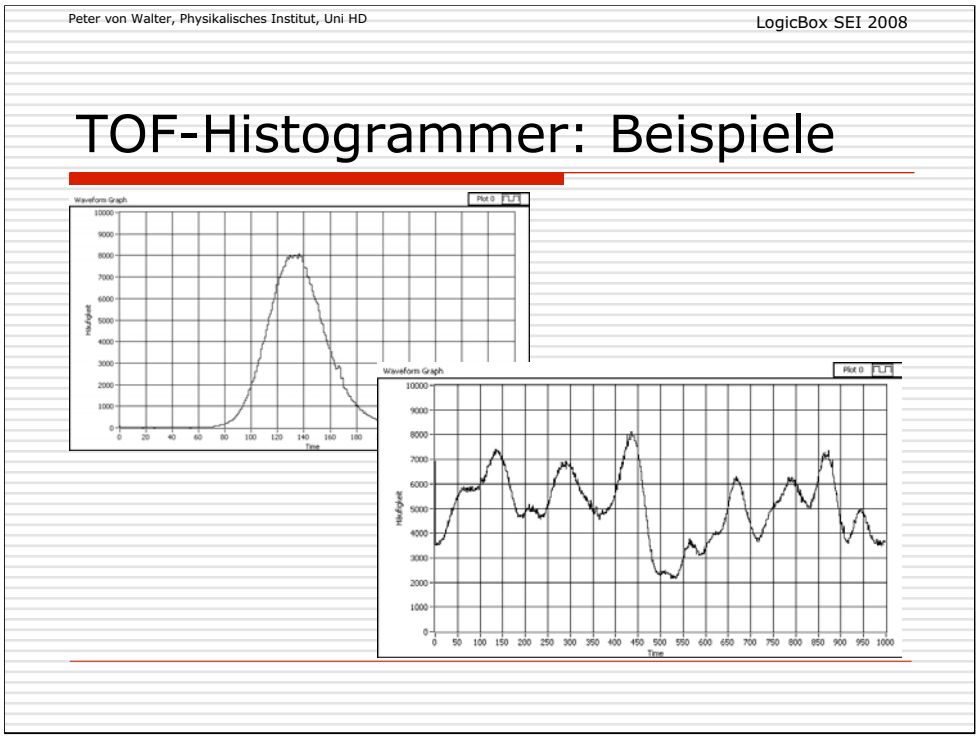


Das Modul misst die Zeit zwischen **TRIG** und einem oder mehreren Signalen an **EVNT** mit einer Auflösung, die durch den Parameter **DWELL** (= DWELL * 10 ns) bestimmt ist. Die Auflösung kann mit 24 Bit (10 ns .. ca.167 ms) beliebig eingestellt werden. Für die gemessene Zeit ist jeweils die positive Flanke der Signale entscheidend.

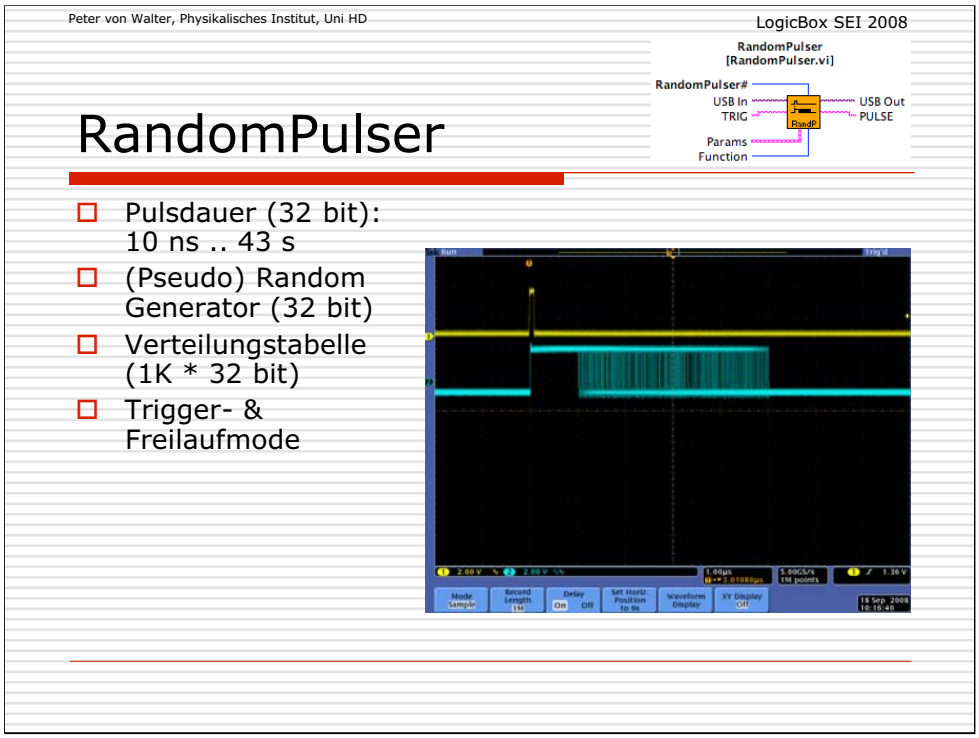
Die Zeitmessung beginnt erst ab dem einstellbaren 16Bit-Parameter **OFFSET** (= OFFSET * DWELL * 10 ns) und wird über die Speichertiefe (= 1024 Kanäle) durchgeführt. Während dieser Zeit kann auch ein mehrfaches Eventereignis auftreten, das falls es nicht in den gleichen Zeitkanal fällt, erfasst wird!

Ein Flag **Retrigger** bestimmt, ob bei vorherigem neuen Trigger, die Messung neu gestartet oder unterdrückt wird.

Die Zeiten werden ohne Totzeit sofort in ein **Histogramm**-Memory (maximale Eventanzahl =2**(16+10) = ca. 67 Mio) einsortiert und können zum beliebigen Zeitpunkt mit einer gewählten **Länge** ausgelesen werden.

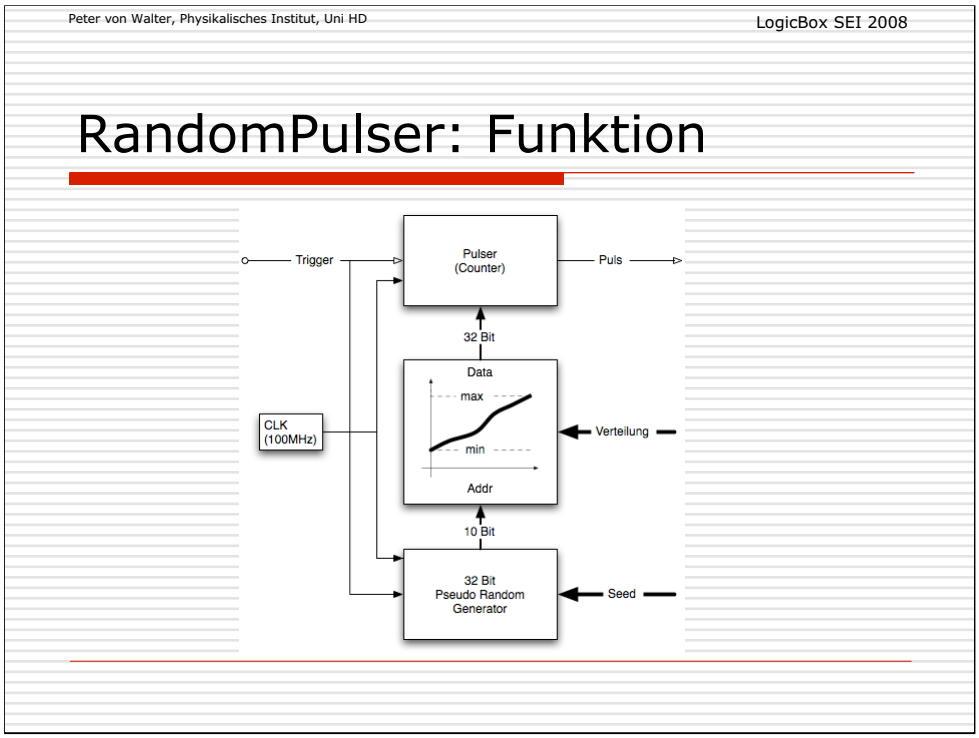


Einige Beispiele von Häufigkeitsverteilungen in Experimenten.

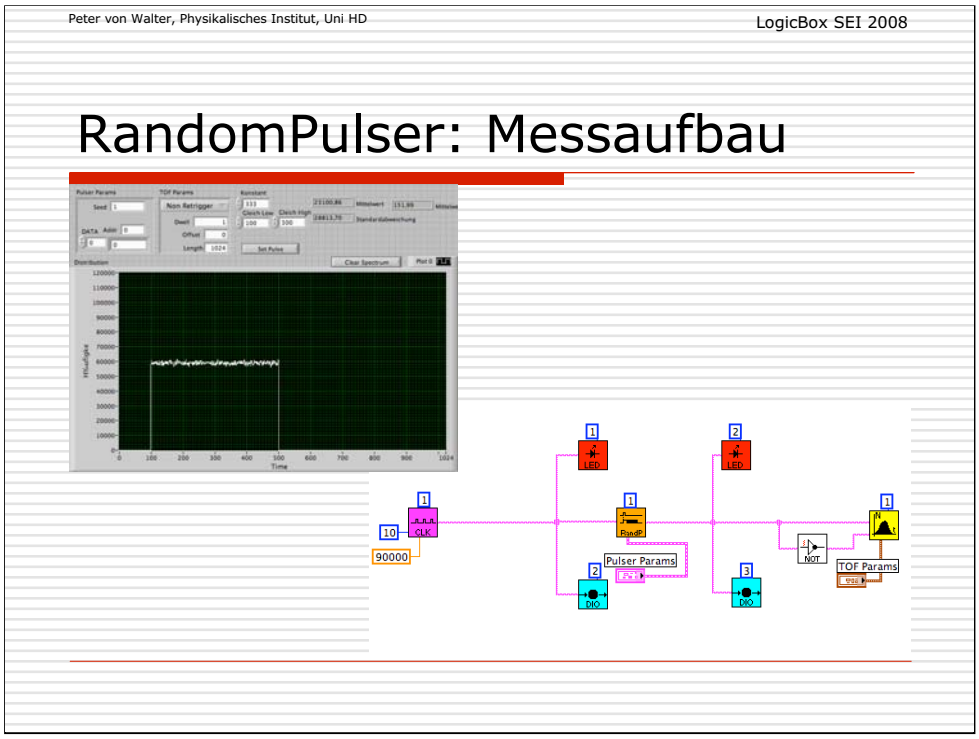


Für das Testen von Auswerteschaltungen an Detektoren ist ein Pulsgenerator mit variabler bzw. zufälliger Pulsdauer vorteilhaft.

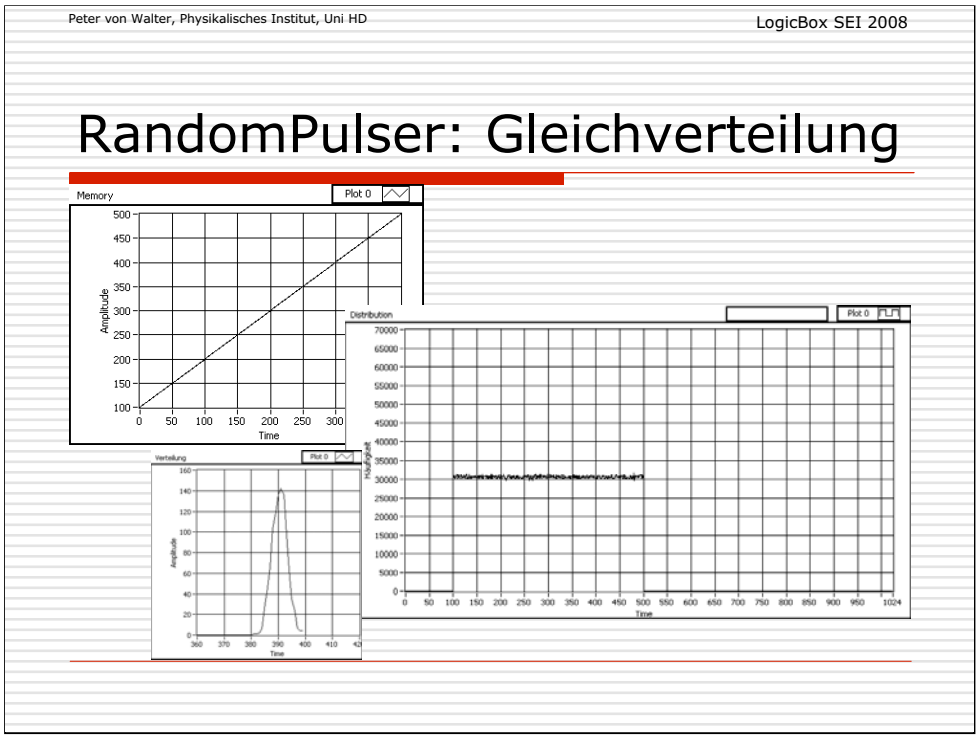
Die Verteilung der Pulsdauer kann über eine Verteilungstabelle weitgehend beliebig bestimmt werden.



Durch den Trigger wird über einen Pseudo-Random-Generator eine zufällige Adresse (10 Bit) generiert, die über ein ladbares Memory die eigentliche Pulsdauer bestimmt. Mit dieser Zahl wird der Pulsgenerator gestartet. Nach Ablauf des Pulses kann beliebig über einen Trigger ein erneuter Puls gestartet werden oder der Pulsausgang wird (invertiert) mit dem Trigger verbunden um einen freilaufenden Pulser mit variabler Zeitdauer zu realisieren.



Der Messaufbau zeigt das LabVIEW-Programm mit einer Clock für den Trigger des RandomPulsers und den TOF-Histogrammer zur Auswertung und Darstellung der Zeitverteilung.

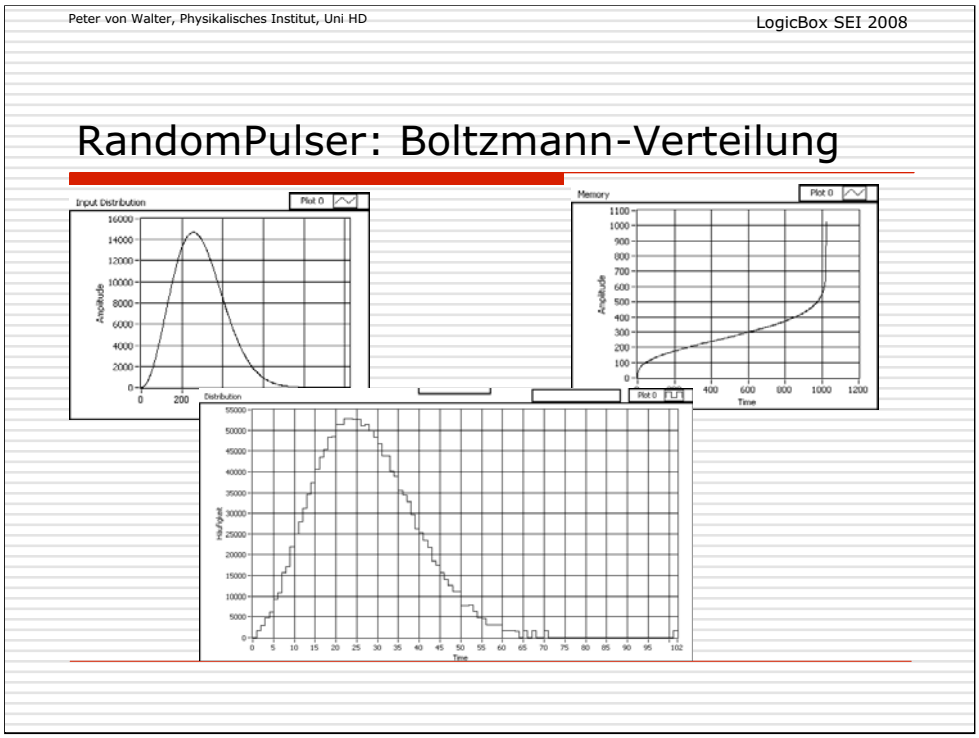


Beispiel für Gleichverteilung der Pulszeiten von 1 .. 5 us:

-Links oben: Werte im Memory

-Rechts unten: Histogramm der Pulszeiten

-Links Unten: Verteilung der Variation der Häufigkeiten aus dem Histogramm

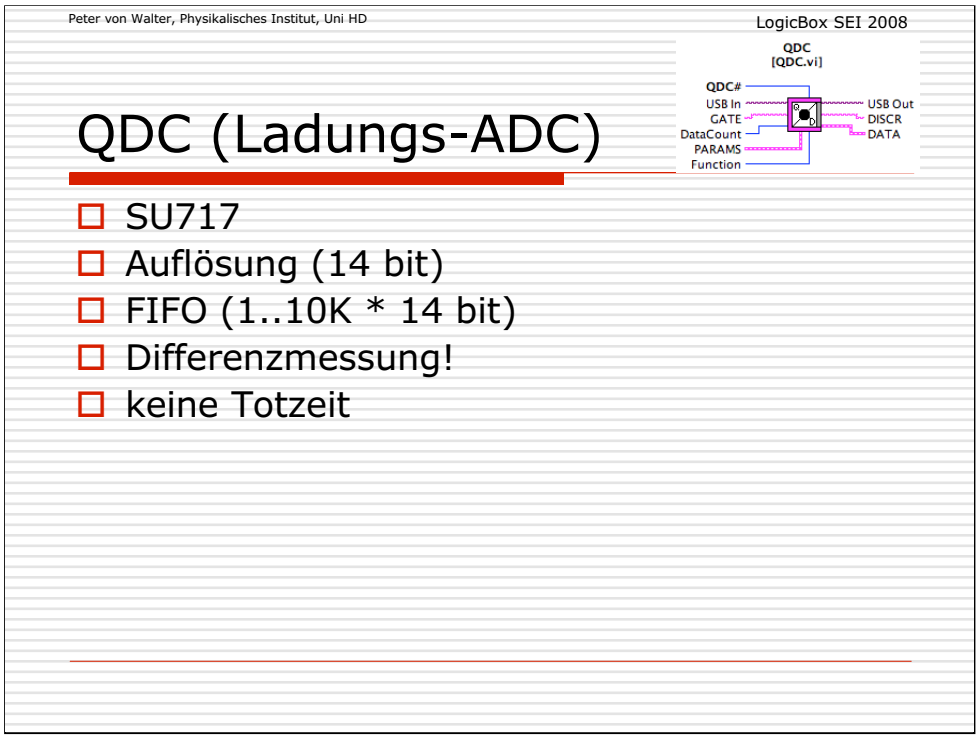


Beispiel für Boltzmann-Verteilung:

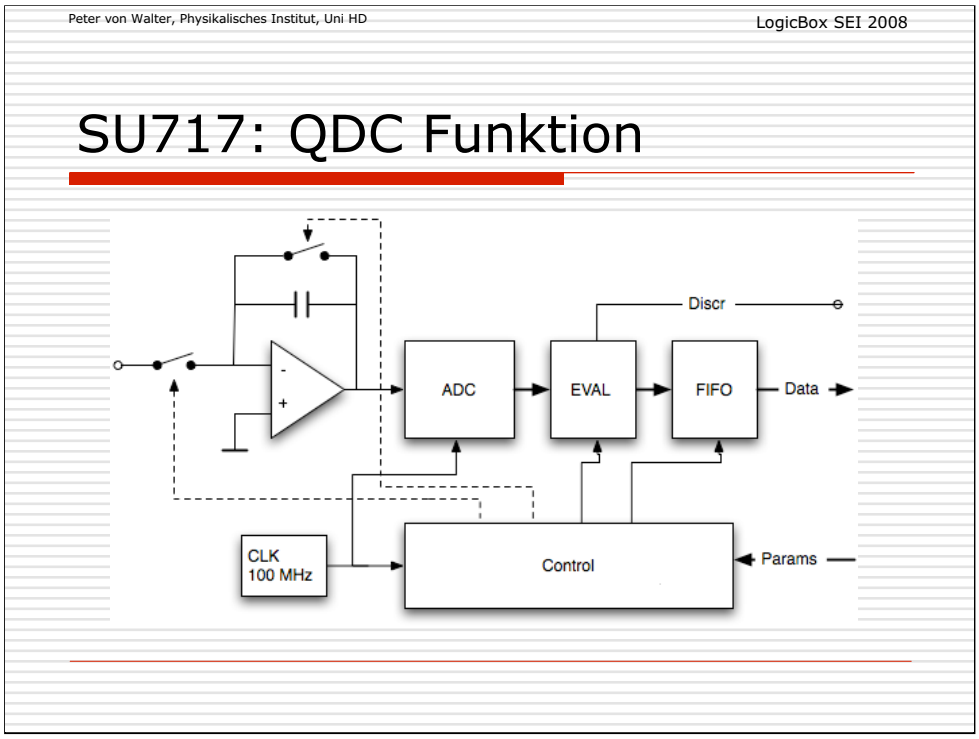
-links oben: Ausgangsfunktion

-Rechts oben: Werte im Memory

-Unten: Erzeugte Verteilung

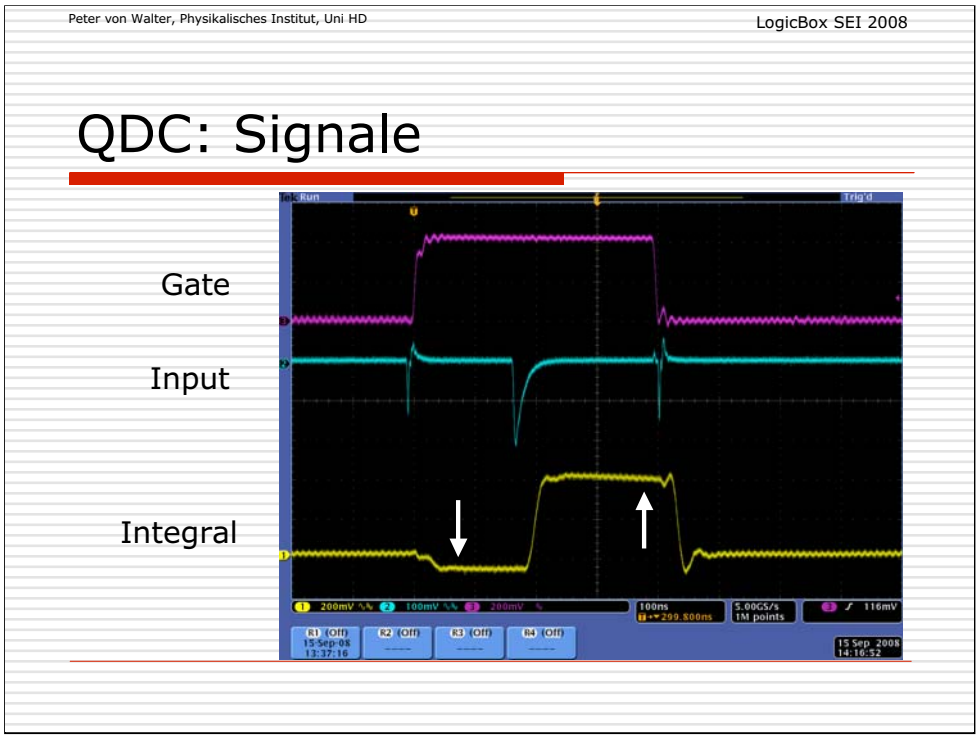


Eine neue aktuelle Entwicklung zur Messung von Ladungsimpulsen aus einem Photodetektor.



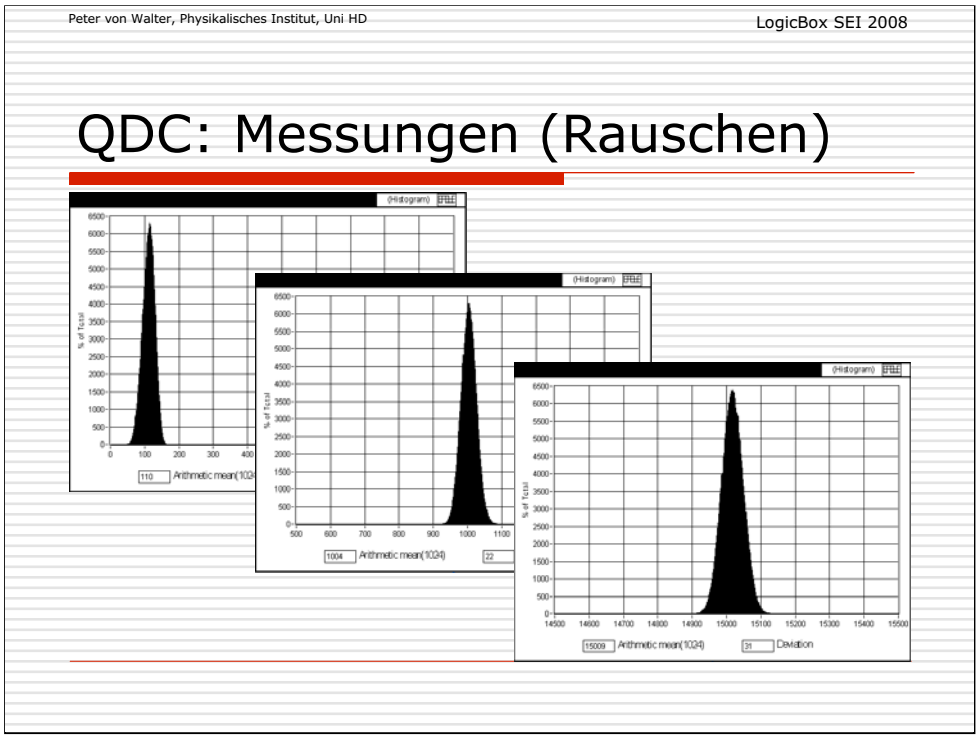
Funktions-Blockschaltbild des QDC:

Die Ladungen am Eingang werden über einen geschalteten Integrator aufgesammelt und die Integrationsspannung über einen schnellen ADC (100 MHz) gemessen. Durch mehrmaliges Messen über den typischen Integrationszeitraum von hier 300 ns können einer einer nachgeschalteten Verrechnungsschaltung bestimmte Fehler unterdrückt werden. Letztlich werden die Daten dann für das Auslesen in einem FIFO abgespeichert.



Typische Signalformen mit den typischen Fehlern durch das Schalten verursacht.

Der Fehler kann durch zweimaliges Sampling (und z.B. durch Differenzbildung) an bestimmten Stellen verringert werden.



Das Gesamtrauschen wird durch die unterschiedlichen Signalhöhen beeinflusst.

LogicBox: Zukunft

- Basiskarte
  - Virtex 4,5 (.. 50 fache Kapazität)
  - Mehr Submodule (8)
  - ...
- Anwenderspezifische Submodule
  - incl. AD-Wandler, DA-Wandler
  - Speicher
  - Interfaces
  - ...
- Anwenderspezifische Firmware
  - Entwicklungskits
  - ...

Durchblick?

Eine Weiterentwicklung der LogicBox ist in mehreren Bereichen möglich.

Letztlich werden diese durch speziellere und weitergehende Anforderungen von den Anwendungen her bestimmt.

Anmerkungen zum Large Hadron Collider LHC

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SEI Tagung IPP Greifswald 22. – 24. 9. 2008

Zusammenfassung
Der größte Beschleuniger der Welt, der Large Hadron Collider (LHC) hat am 10. 9. 2008 am CERN bei Genf seinen Betrieb aufgenommen. Es werden einige Anmerkungen aus den verschiedenen Bereichen gemacht und im Vortrag Bilder dazu gezeigt.

LHC

Zu Beginn des Universums vor 13.7 Mrd. Jahren war das Universum in einem kleinen Punkt konzentriert. Diesen Zustand wollen wir mit dem LHC erforschen. Die Kollisionen der Protonen beim LHC beschreiben das Universum zu einem Zeitpunkt von einem Hundertsten eines Milliardstel einer Sekunde (10^{-11} s) nach dem Urknall.
Ein wesentliches Ziel des LHC ist die Suche nach dem Higgs Teilchen. Dieses Teilchen erzeugt ein Feld, das anderen Teilchen Masse gibt. So ähnlich, wie die Luft einem Helium Ballon eine negative Masse gibt.
Die ersten Ideen, einen LHC zu bauen, gehen auf die Konferenz in Lausanne, 1984, zurück.
Während einer Sekunde überschreiten die Protonen 66000 mal die französich-schweizer Grenze.
Die Strahlen werden 10 h in LHC gespeichert. Dabei legen sie eine Entfernung von 10 Mrd. km zurück. D. h. einmal zum Neptun und zurück.
Bei einer Kollision ist die Temperatur in einem winzigen Volumen eine Mrd. mal heißer als im Innern der Sonne.
Die Temperatur für die Magnete liegt bei -271 Grad Celsius (1.9 K). He wird bei diesen Temperaturen supra-flüssig. Supra-flüssiges Helium kann die Wände hochkriechen und entweichen.
Die Filamente der supraleitenden Magnete sind 10 mal dünner als ein Haar. Aneinandergereiht reichen sie bis zu Sonne und zurück. Es wurden 1232 supraleitende Magnete gebaut. 15 m lang. 35 t schwer. Insgesamt sind 1800 Magnete eingebaut.
Wenn man den LHC mit normalleitenden Magneten gebaut hätte, dann hätte er 120 km Umfang.
Dank moderner Telekommunikation kann man vom Fermilab in Chicago den Betrieb bei LHC verfolgen.
9000 Physiker mit 100 Nationalitäten benutzen die Einrichtungen vom CERN. Das ist die Hälfte der Teilchenphysiker.
Daten können mit einer Rate von 6.25 GBit/s nach Los Angeles geschickt werden. Das ist 10000 mal schneller als typische Hausinstallationen.
Pro Jahr werden 15 Mill. Gigabyte Daten genommen. Das füllt 3 Mill. DVDs, die aufeinandergestapelt so hoch sind wie der Mont Blanc.
Während einer Sekunde finden 600 Mill. Zusammenstöße statt.
Ein 1 CHF Geldstück würde nach Beschleunigung 33 kg schwer sein.
Die Energie des LHC Strahls entspricht der Energie eines TGV bei 150 km/h.
Das Strahlgrab wird beim Auftreffen des Strahls auf 800 Grad Celsius erhitzt.

Baukosten: 6 Mrd.CHF, 3.5 Mrd. EUR.

ATLAS

Einer der Detektoren von Atlas war so empfindlich, dass er von Kalifornien bis Genf in einem Sitz der 1. Klasse flog. Die Sitze der 2. Klasse waren zu eng.
Beim Transport einer 6 m hohen Komponente war der Weg durch eine neue Brücke versperrt. Das Teil wurde mit einem Autokran über die Brücke gehoben.
Die Pixel Detektoren arbeiten wie eine Digitalkamera. Typische Detektoren haben 80 Megapixel.
Die Genauigkeit der Aufstellung der Detektoren beträgt 0.05 – 0.3 mm. Das ist die Dicke eines Haares.
Die Bewegungssensoren bei Atlas sind so genau, dass sie am 26. 12. 2004 Unregelmäßigkeiten registrieren. Diese hingen mit dem Erdbeben in Sumatra und dem anschießenden Tsunami in Indonesien zusammen.
Die Energie, die in den ATLAS Magneten gespeichert ist, entspricht der Energie von 4000 Fahrzeugen bei einer Geschwindigkeit von 100 km/h. 92 km Kabel wurden in den Magneten verbaut.
Die Toroidspulen sind 25 m lang.
In die Kaverne von Atlas passt der Triumpfbogen von Paris. Sie ist 53 m lang und 35 m hoch. Sie wurde zunächst nur 12 m tief ausgegraben. Dann wurde eine Betondecke installiert, die an 38 Ankern von 25 m Länge befestigt ist.
60 m² Si Streifendetektoren. Steifen sind dünner als ein Haar.
Kosten von ATLAS: 550 Mill. CHF (330 EUR)

CMS

Die Hydraulik und Steuerung zum Herablassen der schweren Teile (1920 t) in das CMS Experiment (100 m tief) werden in Südafrika benutzt, um das Dach des Stadions für die Weltmeisterschaft 2010 anzuheben. 5 Jumbo Jets wiegen 1920 t.
Die Energie im CMS Magneten könnte 18 t Gold schmelzen. Der CMS Magnet hat 15 m Durchmesser.

Im CMS Experiment sind 1400 Muonkammern aus 15 Ländern eingebaut.
Einige Blei-Wolfram Kristalle in CMS sind so groß wie eine Kaffeetasse und wiegen 1.5 kg. 77 000 Kristalle wiegen soviel wie 20 Elefanten.
Messing enthält Fragmente von Supernovae Explosionen. Schwere Elemente wie Kupfer, Zink oder Blei in Messing wurden dabei erzeugt.
Über eine Millionen Messingkapseln aus Waffen der russischen Flotte wurden eingeschmolzen und zu Detektor Komponenten verarbeitet.
Die Füße von CMS tragen den Detektor von 12 000 t Gewicht. Das ist mehr als das Gewichts des Eifelturms.
Die schweren Teile von CMS können auf einem Luftkissen bewegt werden.

LHCb

Ein Detektorteil beim LHCb Experiment ist so empfindlich, dass elektronische Verbindungen zerstört werden könnten, wenn eine Nadel auf den Detektor fällt.

Alice

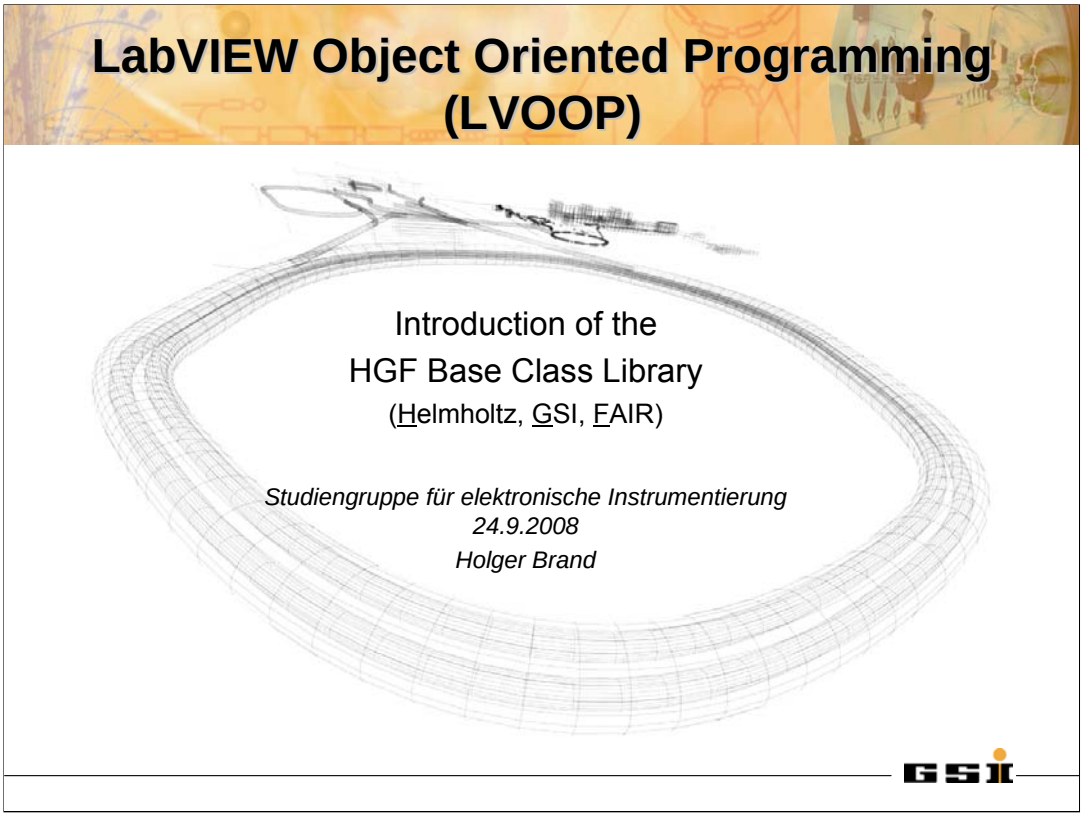
Der Magnet ist 16 m hoch. Er wiegt 8100 t.
Genauigkeit des Pixeldetektors ist 0.1 mm.
Ein Streifendetektor enthält 30 000 Streifen.

Kosten: 70 Mill. EUR
Die Türen des Alice Experiments biegen sich im Magnetfeld durch.

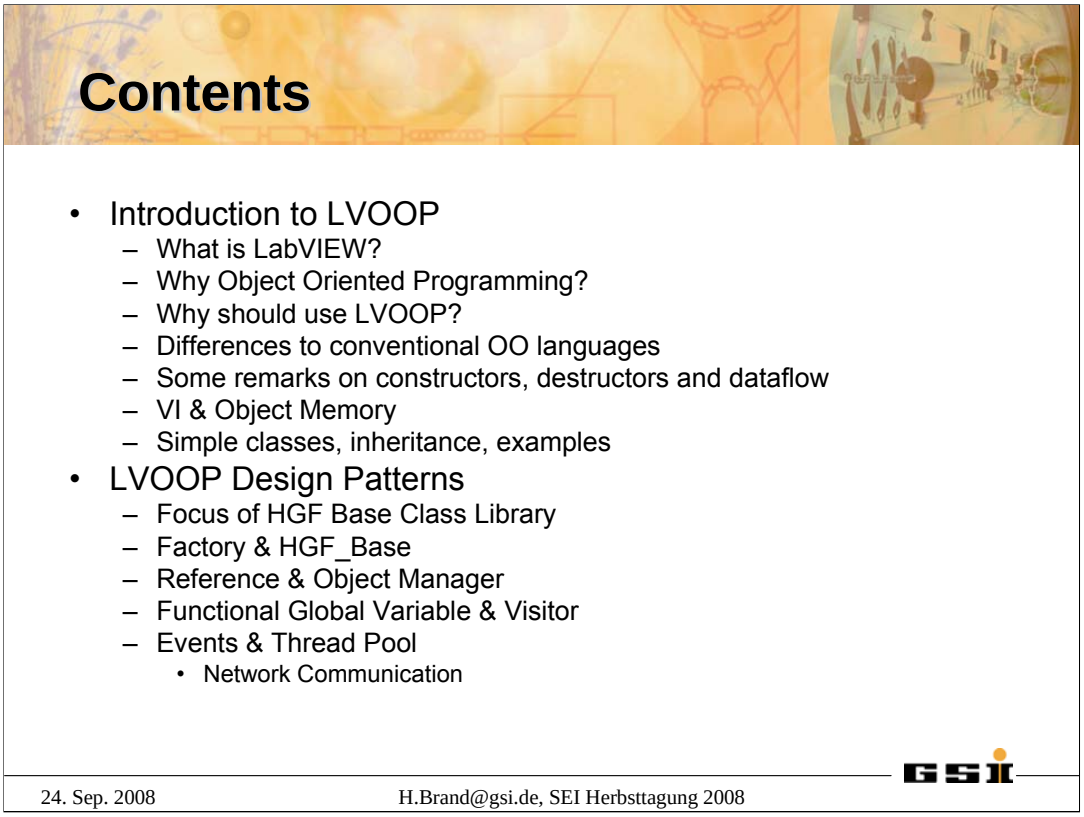
Am Genfer See wurden Bilder über den LHC mit den vier Experimenten ausgestellt. Die Aufnahmen stammen von Peter Ginter. Das Bild zeigt eine Zusammenfassung.

Auf der Rückseite der Bilder waren Texte, die ich übersetzt und oben benutzt habe. Links im Bild sieht man einen Fußball von 15 m Durchmesser. Dieser war mit Helium gefüllt und schwebte über der Fontäne des Genfer Sees anlässlich der Fußball Europameisterschaft 2008.

notzbericht080924.doc



Some comments are taken from http://zone.ni.com/devzone/cda/tut/p/id/3573 and http://zone.ni.com/devzone/cda/tut/p/id/3574.



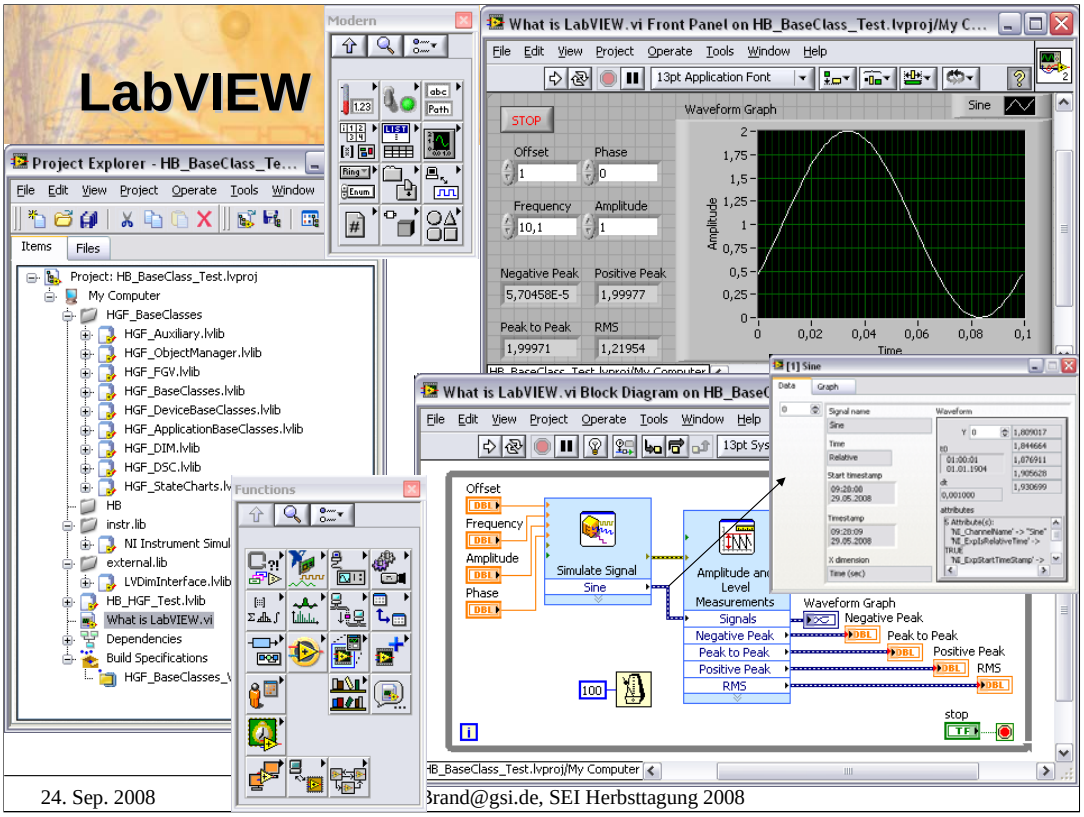
The first part of the talk will briefly introduce LabVIEW, discuss the usage of object oriented software design and point out the differences to conventional object oriented programming languages.

The second part of the talk will focus on LVOOP Design Patterns that enables the usage of LabVIEW objects as entities. The HGF Base Class library contains an implementation of important design patterns with respect to the dataflow paradigm.

What is LabVIEW?

- LabVIEW is a development environment
  - For development of Measurement- , Automation-, Test- and Control Systems.
  - It includes an advanced math and analysis library.
  - Provides interfaces to DAQ, many field busses, network communication, ActiveX, .Net, DLL, etc.
- LabVIEW is a graphical programming language
  - Inherent multithreaded with easy to use synchronization methods
  - **VI**: Virtual Instrument consists of frontpanel and blockdiagram
  - **subVI**: VI to be used as function
  - **Express VI**: configurable subVI
- LabVIEW Modules and Add-Ons extend the base functionality
- Refer to http://www.ni.com/labview

This transparency briefly summarizes LabVIEW and its features.

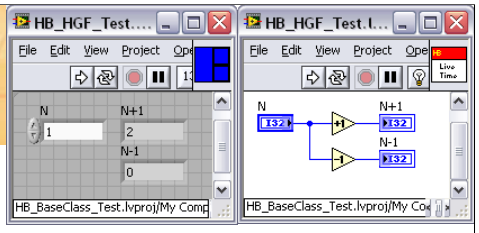


This transparency presents an impression of LabVIEW to be used for oral explanation.

Left hand side shows the Project Explorer it includes VIs, libraries, hardware configuration and build specifications as well as other data types in a logical view.

The right hand side display the frontpanel and blockdigram of an example VI together with the corresponding controls and functions palettes. The frontpanel contains controls and indicators that form the graphical user interface. The blockdigram contains the graphical program code. Probes can be attached to wires to display the data as it flows through the wire.

Dataflow Paradigm



- LabVIEW is a data flow language
- Data flows from data source to sink.
- It *does not normally have variables*.
  - Wires are not variables.
  - Front panel controls are not variables.
  - Even local or global variables are not scoped or allocated the way variables are in other languages.
- Variables are part of a model that conflicts with data flow.
  - Without variables and a scope defining the lifetime of those variables, construction and destruction are meaningless concepts, and therefore they are left out of the language design.

Therefore: LabVIEW forbid LabVIEW classes in the interface of LV-built DLLs (shared libraries).

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It is most important to understand LabVIEW's dataflow paradigm.

LabVIEW has no variable. Instead, data flows from a data source to data sink. At wire forks the data becomes cloned (copied). Data dependencies define the sequence of program execution. Program sequences that have no data dependencies are executed in parallel. Such independent program sequences are also call threads, especially when they contain loops.

There are several ways how a data source on the block diagram can get data. It can get the data from the corresponding frontpanel control, which could be set manually by the user or via VI-Server from another thread programmatically, or from the calling VI via the corresponding pin of the connector pane when used as subVI.

Why Object Oriented Programming?

- Classes
  - Attribute data encapsulation
  - Methods operating on attribute data
  - Access scope
  - (Multiple-) Inheritance
  - Recipe, how to create objects
- Advantages
  - Well defined public interface
  - Well define responsibilities (class and developer)
  - Easier to debug
  - Better scalability
  - Better maintenance
  - Each **object** can be viewed as an **independent little machine or actor** with a distinct role or responsibility (object by reference).
  - Leads to better software design and architecture (hopefully!)

```
// C++ class example
#include <iostream>

using namespace std;

class CRectangle {
private:
  int x, y;
public:
  void set_values (int,int);
  int area () {return (x*y);}
};

void CRectangle::set_values (int a, int b) {
  x = a; y = b;
}

int main () {
  CRectangle rect;
  rect.set_values (3,4);
  cout << "area: " << rect.area();
  return 0;
 }
```

GSI

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•**Object-oriented programming has demonstrated** its superiority over procedural programming as an architecture choice in several programming languages. It encourages cleaner interfaces between sections of the code, it is easier to debug, and it scales better for large programming teams.

> •From wikipedia:
> The idea behind object-oriented programming is that a computer program may be seen as comprising a collection of individual units, or *objects*, that act on each other, as opposed to a traditional view in which a program may be seen as a collection of functions, or simply as a list of instructions to the computer. Each object is capable of receiving messages, processing data, and sending messages to other objects. Each object can be viewed as an independent little machine or actor with a distinct role or responsibility.

•**Object-oriented programming is claimed** to promote greater flexibility and maintainability in programming, and is widely popular in large-scale software engineering. Furthermore, proponents of OOP claim that OOP is easier to learn for those new to computer programming than previous approaches, and that the OOP approach is often simpler to develop and to maintain, lending itself to more direct analysis, coding, and understanding of complex situations and procedures than other programming methods.

Differences between C++ and LVOOP

C++	LabVIEW
text-based, functional language	graphical, dataflow language
Not required	ultimate ancestor class
constructors	no need
destructors	no need
by reference and by value syntax	by value syntax only
no, class must provide mutation code for data	versioning, automatic data mutation
templates	LabVIEW 8.2 and later does not
pure virtual functions	LabVIEW 8.2 and later does not
multiple inheritance	LabVIEW 8.2 and later does not

OO for LV means strict encapsulation, simple inheritance and dynamic dispatching (virtual methods)

Refer to http://zone.ni.com/devzone/cda/tut/p/id/3574

Comparisson of C++ and LVOOP features

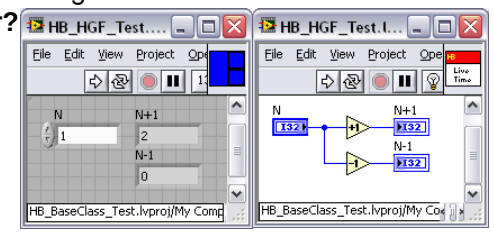
Some remarks

- **LVOOP Naming**
  - A Class is
    - Cluster of private data (C:struct) and
    - Member VIs operating on that data
  - Access scope: public, protected and private VIs
    - Class attribute is always private!
  - Inheritance: Parent (ancestor) and child class
    - **LabVIEW Object** is THE ultimate ancestor class
    - No multiple inheritance
  - Static VI can not be overloaded
  - Dynamic dispatch and overwrite VIs (C++: virtual functions)
    - No overloading! All dynamic VIs with the same name in one inheritance line must have the same connector pane.
  - No friends in this version
- **Default constructor only**
  - Default class attribute values in case of frontpanel control or blockdiagram constant
  - Current attribute data from caller
- **No destructor**

LVOOP FAQ: http://zone.ni.com/devzone/cda/tut/p/id/3573

Scope and Live time (Demo)

- **What is the scope of the C++ integer?**
  It exists from the point it is declared until the closing brace.
- **What is the scope of the LabVIEW integer?**
  Unknown.
  - Until the wire ends?
  - Until the VI stops executing?
  - Until probe is closed?
  - Until front panel closes?
  - …



- **LabVIEW does not have “space scope”. LabVIEW has “temporal scope”.**
  - A piece of data exists as long as it is needed.
  - If it is copied into front panel control, it stays there, even after execution finishes.
  - Copies on the wires exist until the next execution of that wire.
  - Another copy will be made for any probe on the wire.

  - In a pure theoretical data flow language, there would be a separate copy on every individual wire, because every wire is an independent computation unit. Of course, that would be inefficient to actually implement, so **LabVIEW's compiler optimizes the number of copies.**
    But the principle is the same: data lives for a long time, sometimes outliving the program that generated that data.

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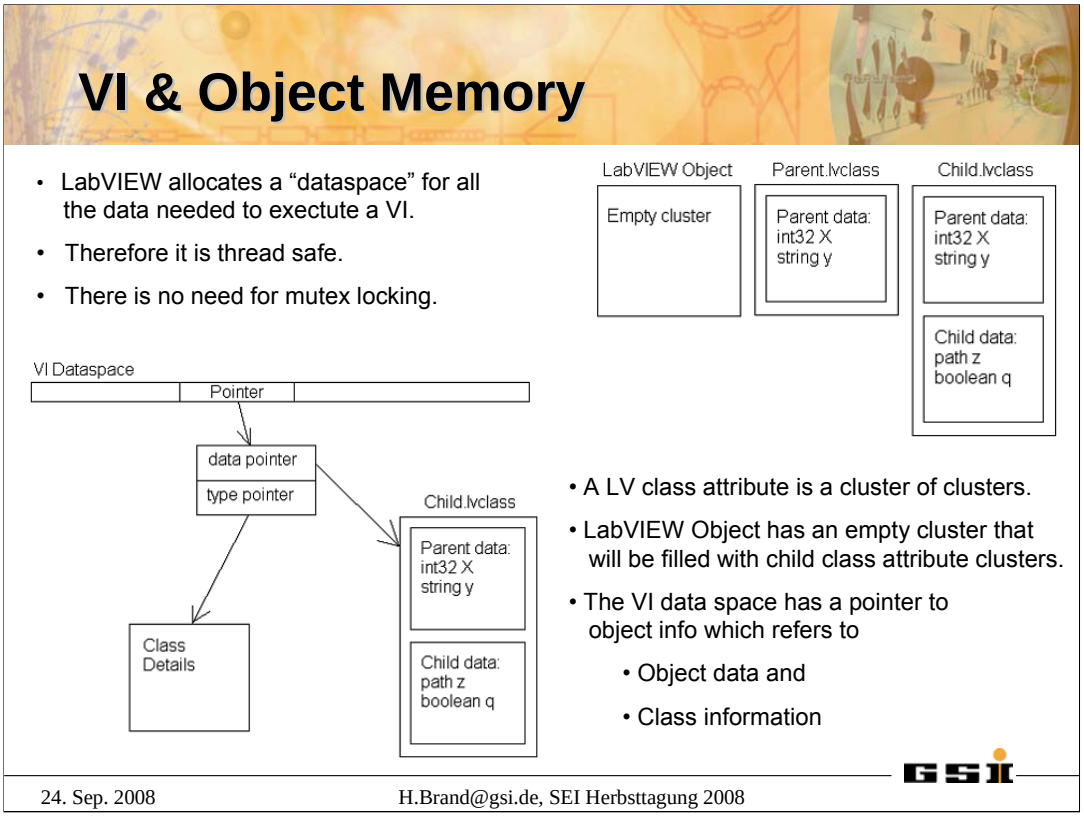
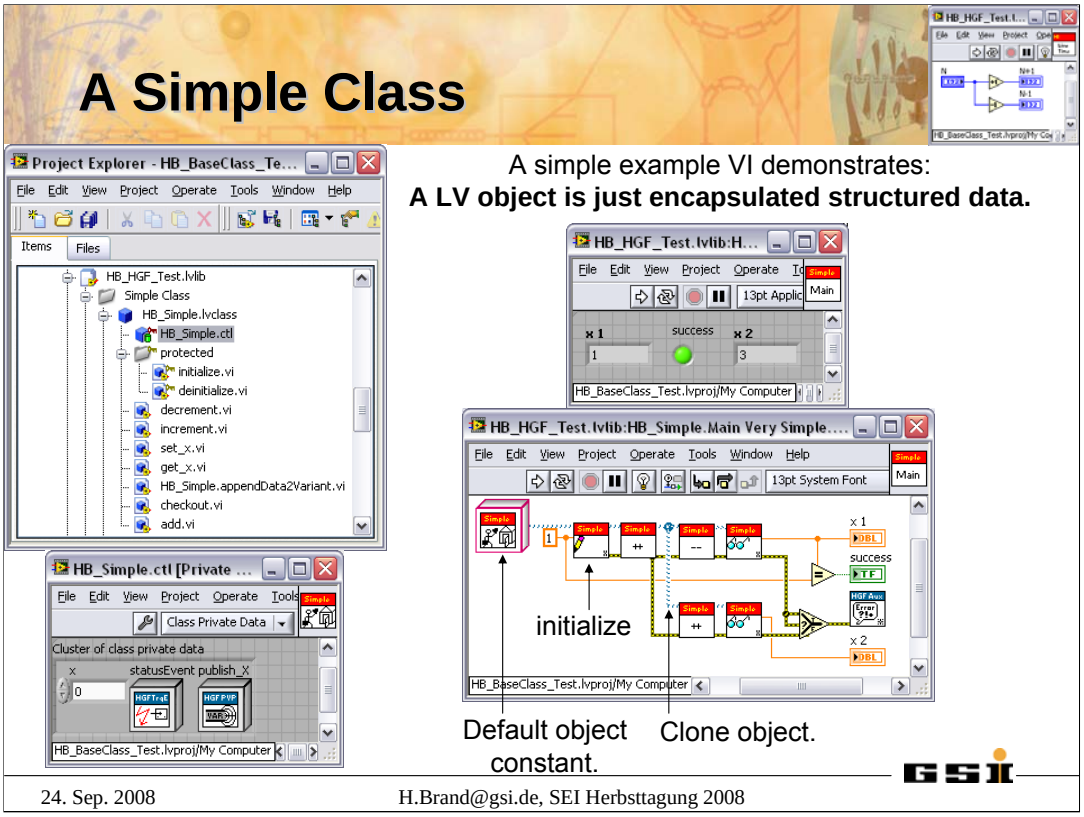
LabVIEW does not have “space scope”. LabVIEW has “temporal scope”. A piece of data exists as long as it is needed and is gone when it is not needed any more. If it is copied into front panel control, it stays there, even after execution finishes. Copies on the wires exist until the next execution of that wire. Another copy will be made for any probe on the wire. In a pure theoretical data flow language, there would be a separate copy on every individual wire, because every wire is an independent computation unit. Of course, that would be inefficient to actually implement, so LabVIEW's compiler optimizes the number of copies. But the principle is the same: data lives for a long time, sometimes outliving the program that generated that data.



When a VI compiles, LabVIEW allocates a “dataspace” for that VI. The dataspace is an allocation of all the data needed to execute that VI. Any thread knows that it is free to write into its region of the dataspace without having to worry that another thread is writing there, so there is no need for mutex locking.

To implement classes, we needed to be able to allocate a class in the dataspace. A wire that is of the parent type must be able to carry data of its own type or any descendent type, so the allocation that we make in the dataspace has to be able to hold any one of the classes. That means that we cannot just allocate these clusters of clusters directly.

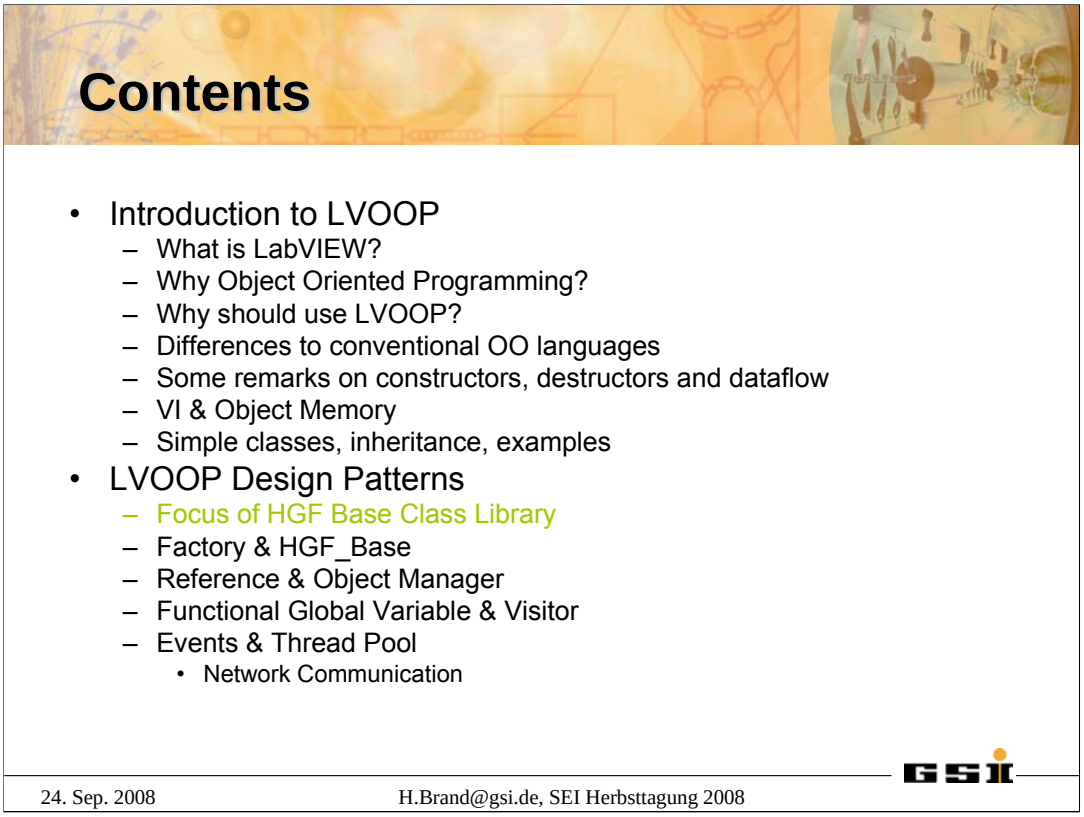
To further complicate the design, an object needs to carry around its class information. An object is a self-aware piece of data. It knows its own type (that is why objects can perform operations such as To More Specific Class and dynamic dispatching). The class information has to be a part of the object at some point. Some helper VIs are available, but not on the functions palette: vi.lib\Utility\LVClass, to be extended with new LabVIEW versions.



HB_Simple class will be used as example class to demonstrate the usage of different design patterns.

The example VI show that a LabVIEW object is just encapulated data. Compere with the simple VI in the upper right corner.

The attribuite x of the default object of class HB_Simple becomes initialized with 1, the default value is defined in the *Class Private Data.ctl*. After incrementing x the object becomes cloned at the wire fork. The upper thread then decrements x and compares the current value with the initialization value. The lower thread increments x once more. The resulting values are displayed in the frontpanel indicators x 1 and x 2. The difference is two as expected with respect to the dataflow paradigm.



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LVOOP Design Patterns

http://en.wikipedia.org/wiki/Design_pattern_%28computer_science%29

- In software engineering, a **design pattern** is a general reusable solution to a commonly occurring problem in software design.
- A design pattern is not a finished design that can be transformed directly into code. It is a description or template for how to solve a problem that can be used in many different situations.
- Object-oriented design patterns typically show relationships and interactions between classes or objects, without specifying the final application classes or objects that are involved.
- Algorithms are not thought of as design patterns, since they solve computational problems rather than design problems.

- **Since LabVIEW objects follow the dataflow paradigm, many design pattern must be reinvented with respect to dataflow.**

Referenced links from Wikipedia:

Design Patterns: http://en.wikipedia.org/wiki/Design_pattern_%28computer_science%29

Software Engineering: http://en.wikipedia.org/wiki/Software_engineering

Software Design: http://en.wikipedia.org/wiki/Software_design

Code: http://en.wikipedia.org/wiki/Code_%28computer_programming%29

Object-oriented: http://en.wikipedia.org/wiki/Object-oriented

Interactions: http://en.wikipedia.org/wiki/Interaction

Classes: http://en.wikipedia.org/wiki/Class_%28computer_science%29

Objects: http://en.wikipedia.org/wiki/Object_%28computer_science%29

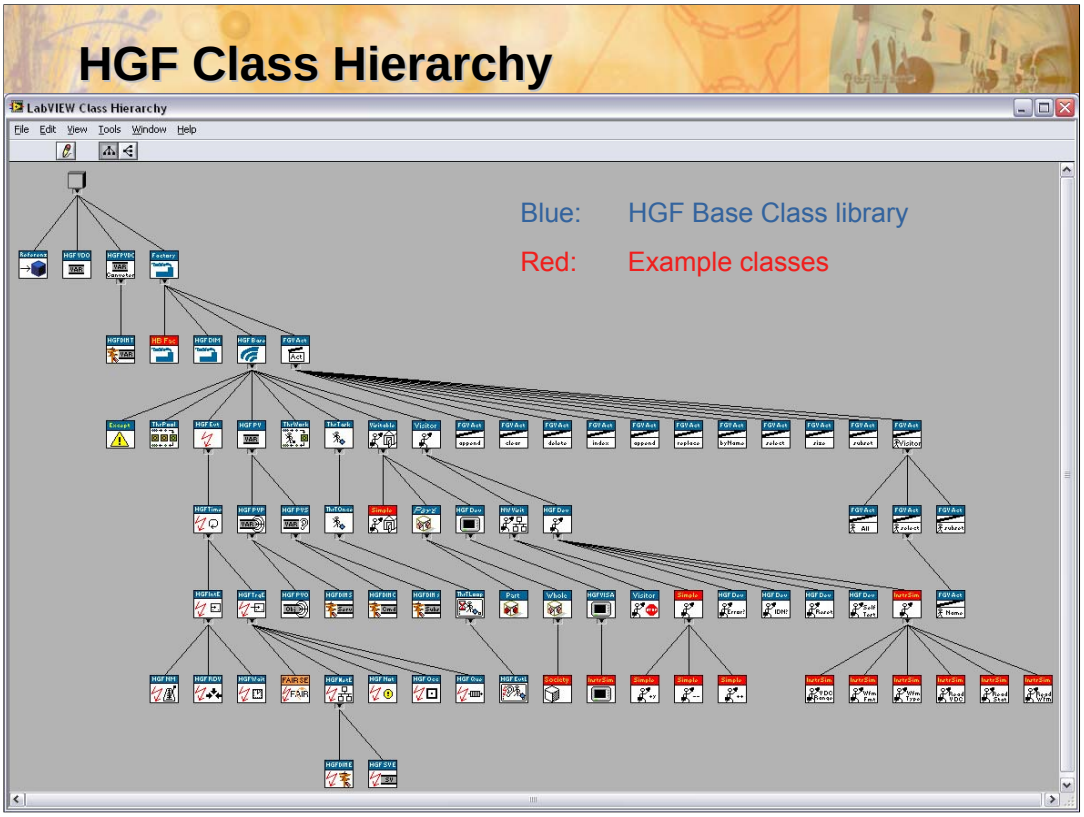
Algorithms: http://en.wikipedia.org/wiki/Algorithms

Computation: http://en.wikipedia.org/wiki/Computation

Design: http://en.wikipedia.org/wiki/Design

Focus of HGF Base Class Library

- How to deal with LabVIEW objects as entities?
  - *Factory*
    - Named objects
    - Constructor and destructor
- How to prevent unintended object wire forks?
  - *Reference, Singleton*
  - Object Manager
  - Functional Global Variable & *Visitor*
- How to deal with Agents?
  - Separation of passive object data and active threads –> *Thread Pool*
  - Event handling
- How to overcome some technical restrictions?
  - Missing class information -> vi.lib\Utility\LVClass
  - Missing overloading -> *Variant*
  - Missing Multiple Inheritance -> *Aggregation*
  - Missing Interfaces -> *Delegation*



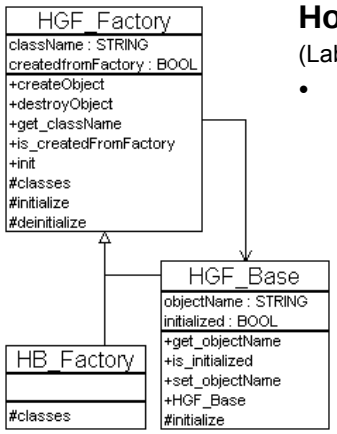
LabVIEW provides a view of the LabVIEW Class Hierarchy which is shown here for the HGF Base Class library. The top gray box is THE *LabVIEW Object* the basic ancestor class. Blue classes belong to the HGF Base Class library. Red classes demonstrate the usage of the HGF Base Classes. LabVIEW provides no UML class diagrams. Only the inheritance tree is shown, but neither associations between classes nor aggregation or composition. For that purpose the UML-Modeler of Endevo can be used, http://www.endevo.se/index.php/en/Produkter_Beskrivningar/Endevo-UML-Modeller-1.2.html.

Contents

- LVOOP Design Patterns
  - Focus of HGF Base Class Library
  - Factory & HGF_Base
  - Reference & Object Manager
  - Functional Global Variable & Visitor
  - Events & Thread Pool
    - Network Communication

The next transparencies will introduce the **Factory** design pattern *HGF_Factory* and the *HGF_Base* class to be used for derived classes that specify objects to be used as entities.

HGF_Factory & HGF_Base



How to create initialized, named objects?

(LabVIEW provides objects with default attribute values only!)

- **HGF_Factory** is a base class
  - It creates initialized objects that remember their class names and whether it was created by a Factory.
  - It defines two dynamic dispatch VIs (virtual methods)
    - *classes*
      - VI that returns a default object of a desired class.
      - To be overwritten by **child factories**.
    - *initialize*
      - VI that uses variant attributes to initialize the default object.
      - To be overwritten by **child classes**.
- **HGF_Base** is the base class for ***Entities***
  - Named object that remembers whether it was initialized.
  - Overwrites the initialize method.

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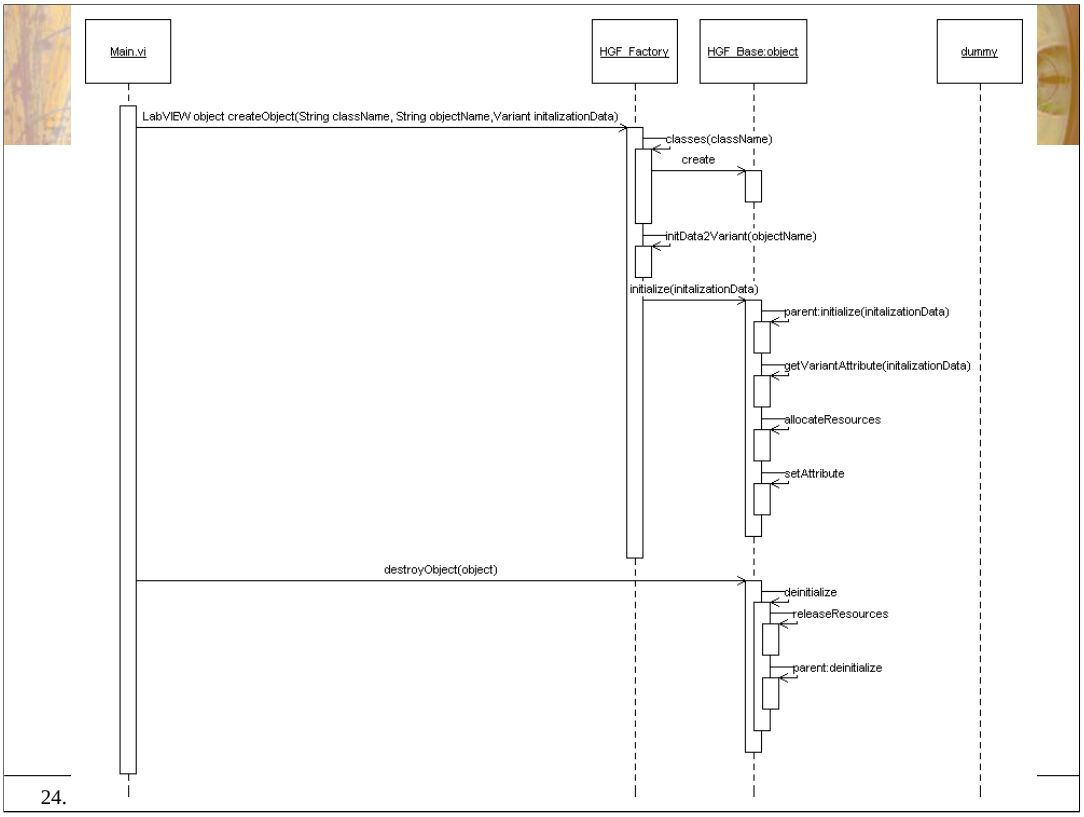
This transparency shows the UML class diagram of the *HGF_Factory* on the left hand side and a description of its features on the right.

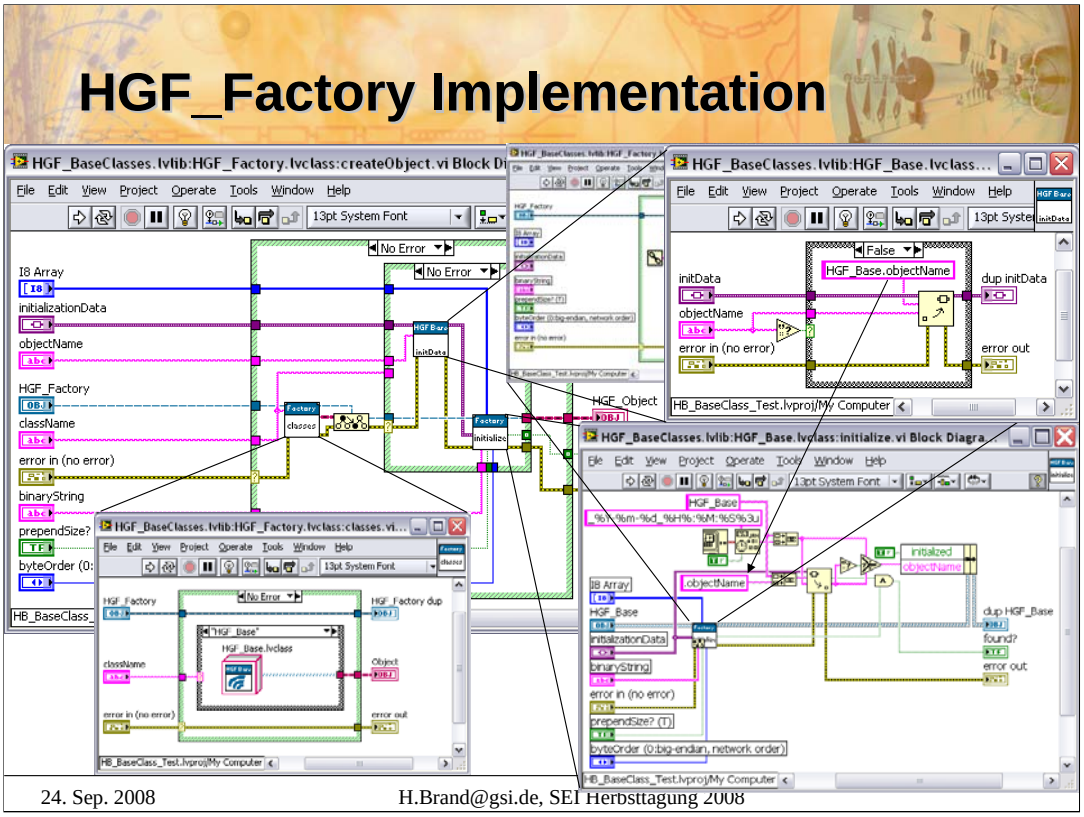
The *HGF_Factory* has an association to *HGF_Base* to provide the object name as input for the *createObject* method for convenience and intuitive interface.

Both classes remember some information which is otherwise not available from LabVIEW, but maybe necessary to know on application level, such as *className*, *createdFromFactory*, *objectName* and *initialized*. For example a framework application, or even the object itself, can query if the object was created by a *HGF_Factory* or whether it was initialized or not.

HGF_Factory provides class constants for all classes that are part of the HGF Base Class library. A developer needs to create his own factory, e.g *HB_Factory*, that overrides the *classes.vi* to provide other class constants to be produced. Classes that inherit from *HGF_Base* have to override the *initialize.vi* method to allocate resources and initialize their attributes.



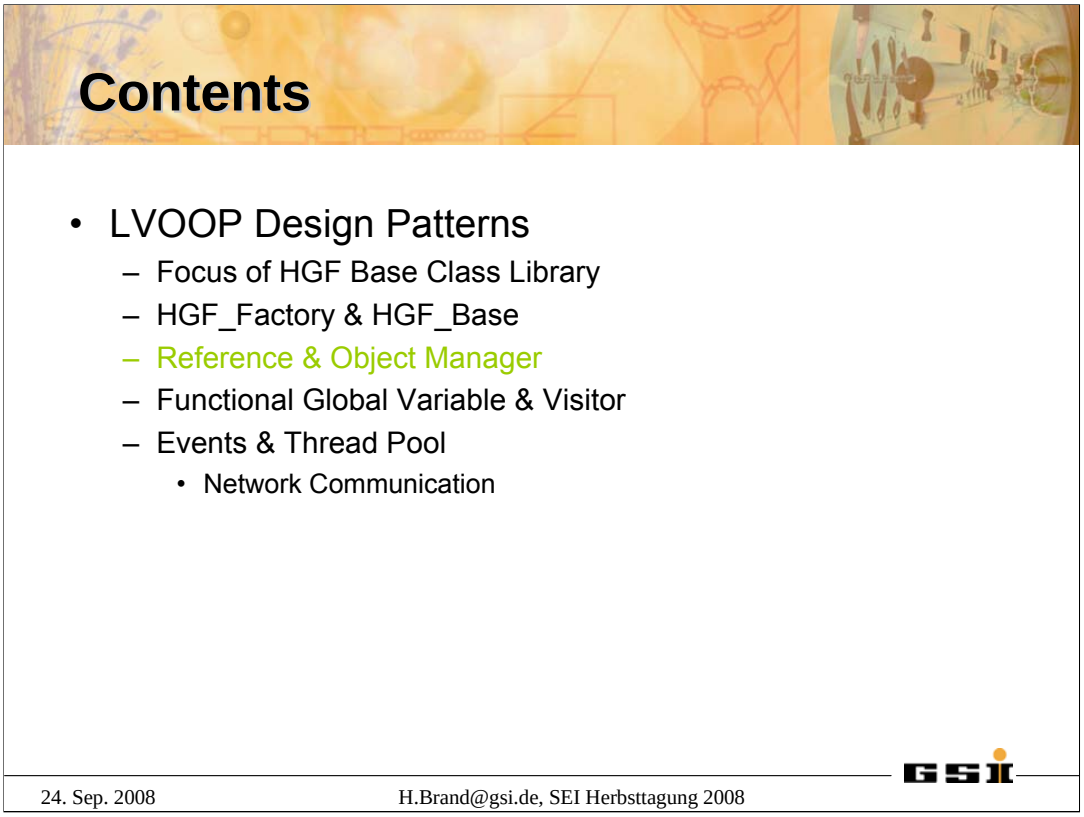
This sequence diagram shows two scenarios. The upper part shows the sequence how an object is created and initialized, the lower how is becomes destroyed.



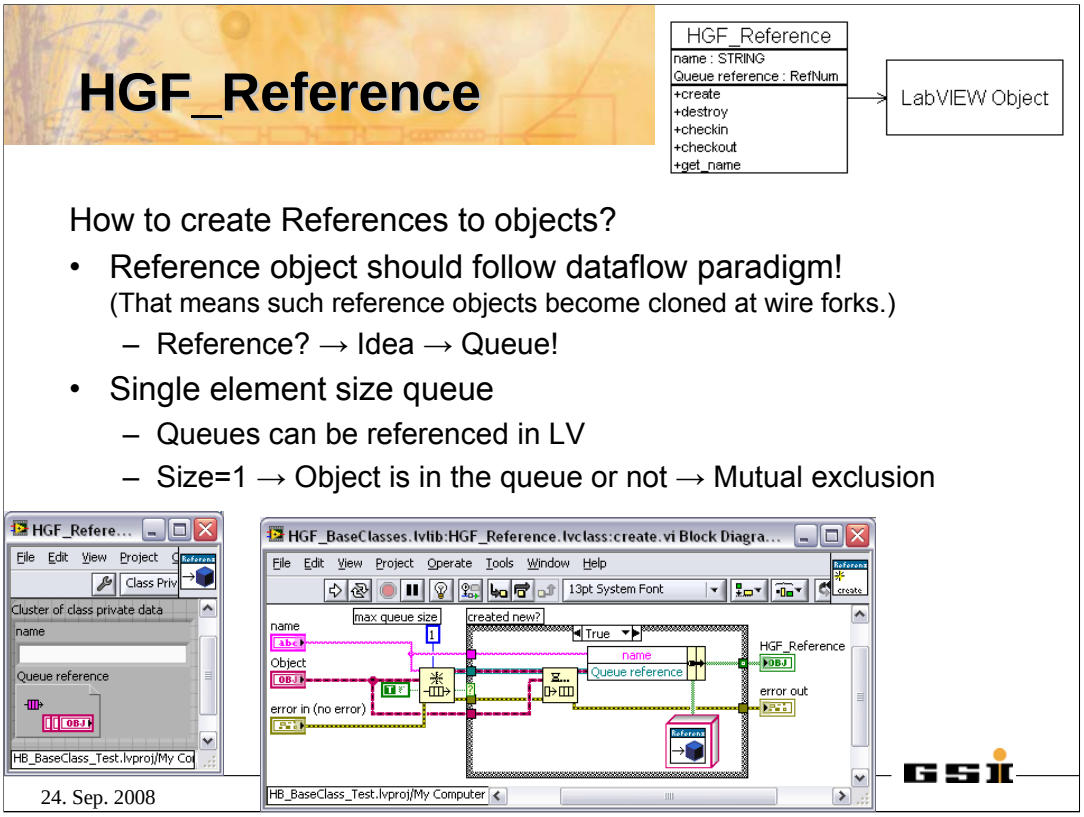
This slide shows the implementation of *HGF_Factory:createObject.vi*.

Since a VI can not be overloaded, we have to face the problem of different initialization parameters for different classes. A variant data type can not only have a value, but also an arbitrary number of attributes of arbitrary types. This feature is used to overcome that problem. To avoid typing mistakes each class provides a method *classname.initData2Variant.vi* which writes specific VI parameters to the corresponding variant attribute. The *classname* prefix is necessary to avoid the VI naming problem. Of course the variant attributes can be also written directly from an application VI, e.g. parsing network data generically.

In a first step the *classes.vi* method is called to create a default object of the desired class. The *objectName* it written to the corresponding variant attribute. Finally the overwrite method *initialize.vi* of objects class is called to initialize itself. It first calls its *parent class:initialize.vi* , which calculates the *className* and remembers whether it was called from the *HGF_Factory*. Then it initializes its attribute values from the corresponding variant attributes. It also indicates that the initialize method was called which is otherwise not possible because the attribute has private scope and no accessor method it provided by the class.

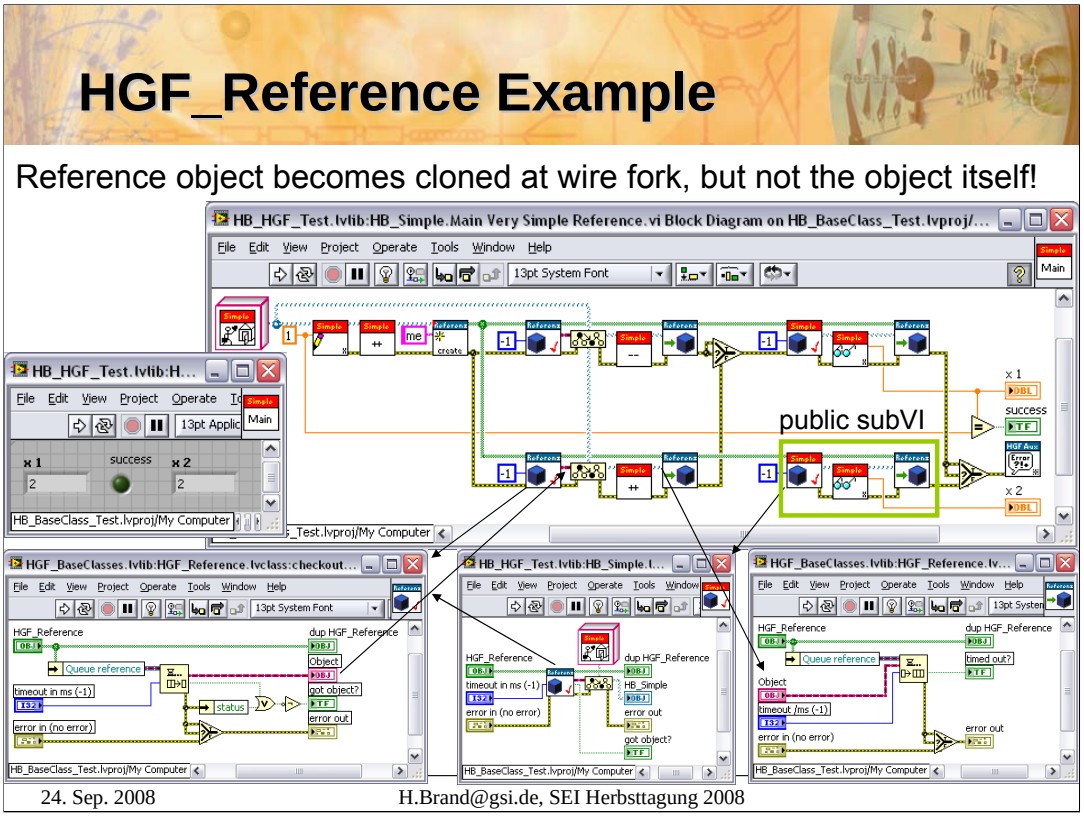


The next transparencies will introduce the **Reference** design pattern, *HGF_Reference*, and the *HGF_ObjectManager* library to deal with LabVIEW objects as entities. Also the **Singleton** design pattern becomes introduced as special case of the Reference pattern.

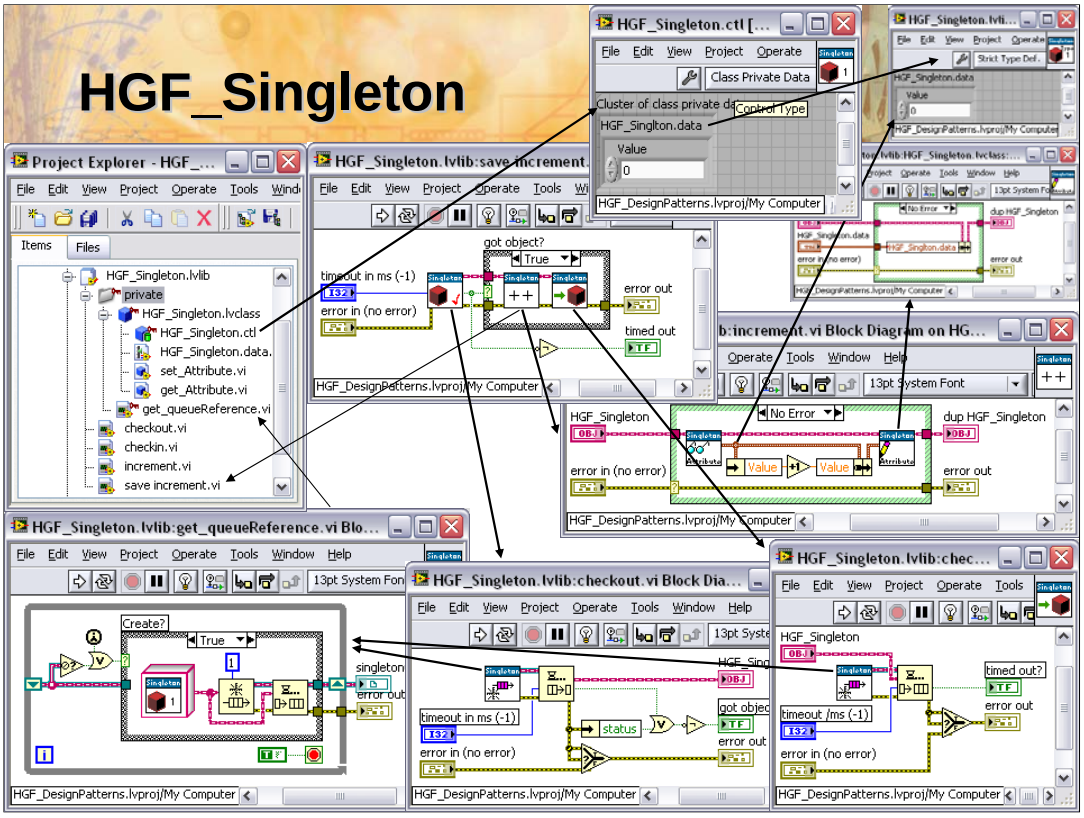


In order to deal with LabVIEW objects as entities we need to develop a helper class since we can not forbid the user to object wires. Such reference objects need to follow the dataflow paradigm. A LabVIEW queue perfectly fulfills that requirements. Queue can be referenced. It is no problem to copy queue references since their contents are not copied. If the queue is single element size the mutual exclusion between different assessors is guaranteed automatically, an object is in the queue or not.

The *HGF_Reference.lvclass:create.vi* creates a new single element sized queue and enqueues the given object immediately. The queue reference is stored in the HGF_Reference attribute which is returned to the caller.

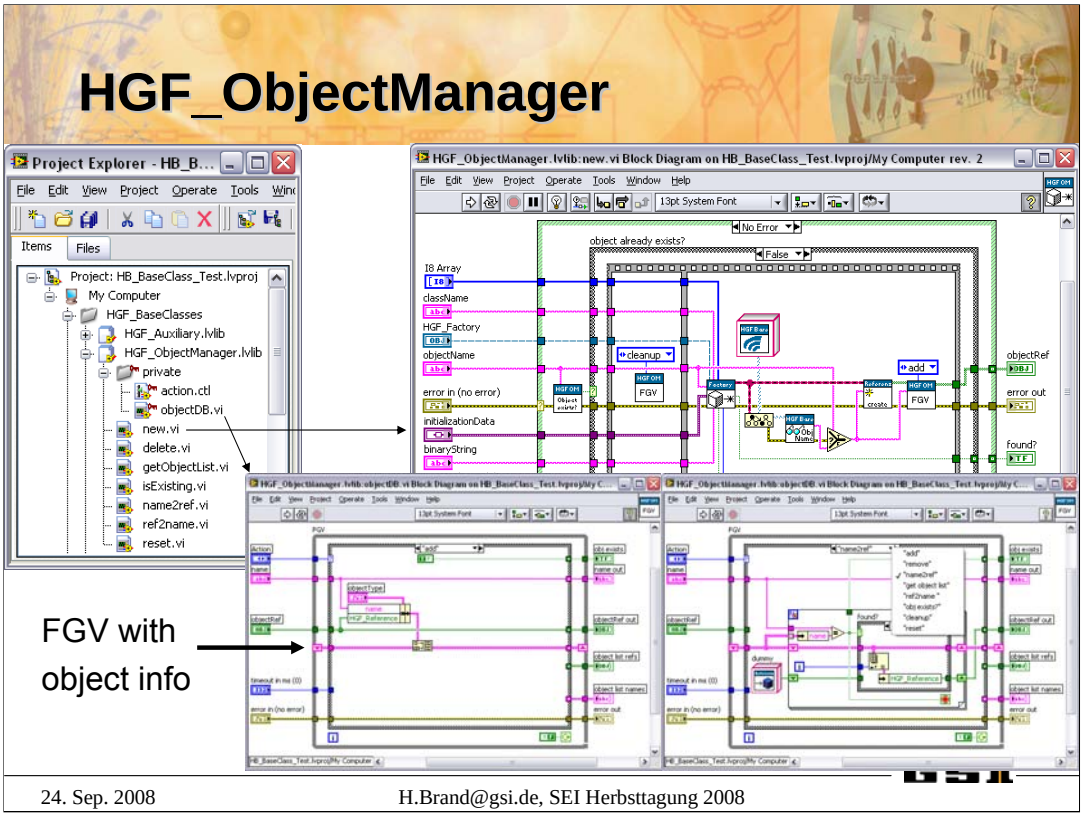


This example shows how to access objects by reference from different threads. It also demonstrates that the LabVIEW object really follows the dataflow paradigm. It flows from the reference queue through the Vis and back into the queue. Of course the developer is responsible to check-in the object after manipulation and to create no clones. The class developer could also decide to declare only those VIs public that already include the check-out and check-in Vis, so the user of the class has no chance to access the object directly, but the reference object only.



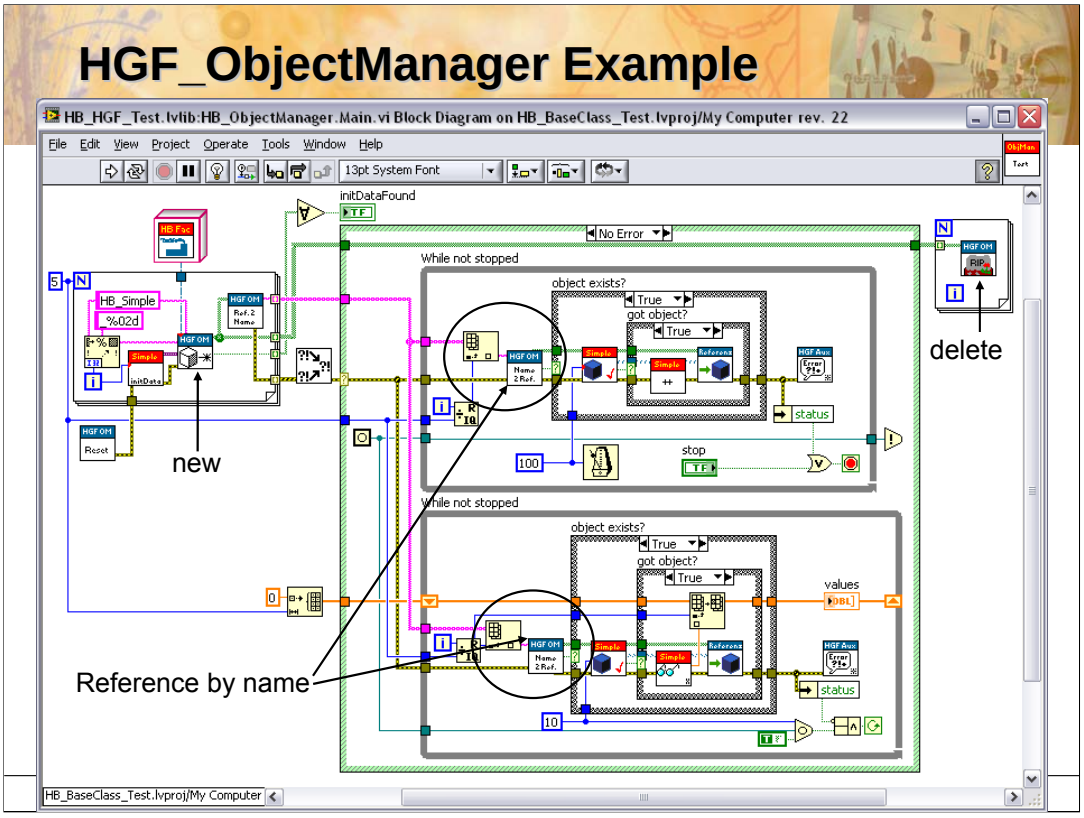
The *HGF_Singleton* is a library that contains a private class and queue reference to ensure that only one instance of that class can be created.

The private class attribute is defined as strict type data cluster. The class provides methods to get and set the attribute data which can be used by public VIs to implement the required functionality. The queue is created once on first call and the default object of class is inserted. The queue reference is stored in an uninitialized shift register (functional global variable) in a private method and is returned on each subsequent call. As a result neither the queue reference nor the object becomes available to the user of the *Singleton*. It is guaranteed that no object clones can be created outside of the library, that means out of control of the *Singleton* developer.



The *HGF_ObjectManager* is a library that maintains a private FGV which contains an array with unique corresponding entries, object reference and object name.

The library provides methods to create new objects and to destroy them. So, there is no way to **accidentally** clone objects. A developer has to checkout an object before he can have access to it. Of course, he has to make sure that he does not create clones and finally check-in the object into the reference again. An example is shown on the next slide.



This example shows how to use the *HGF_ObjectManager* and how to access object by reference or name from different threads. Please make sure that the *HGF_ObjectManager.lvlib:delete.vi* is called for all objects at the end of your program to cleanup all acquired resources.

Contents

- LVOOP Design Patterns
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  - Functional Global Variable & Visitor
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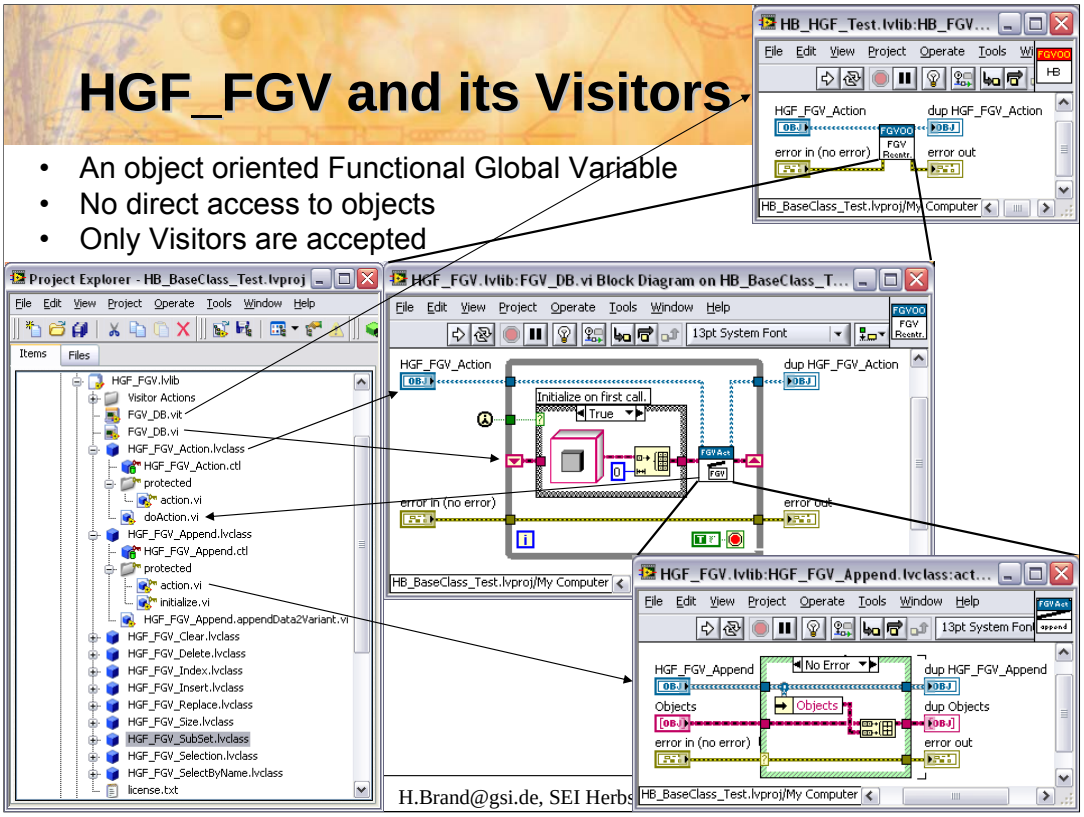
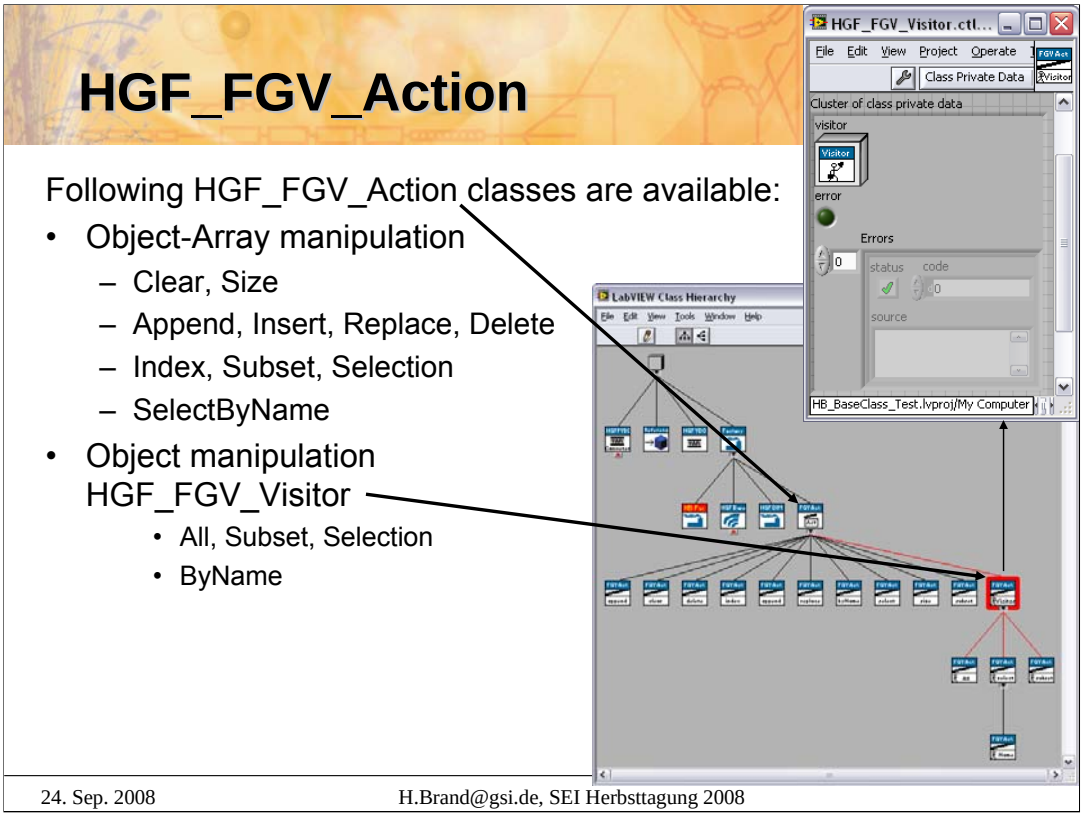
    - Network Communication

The next transparencies will introduce the **Functional Global Variable** design pattern, *HGF_FGV*, and the **Visitor** design pattern.



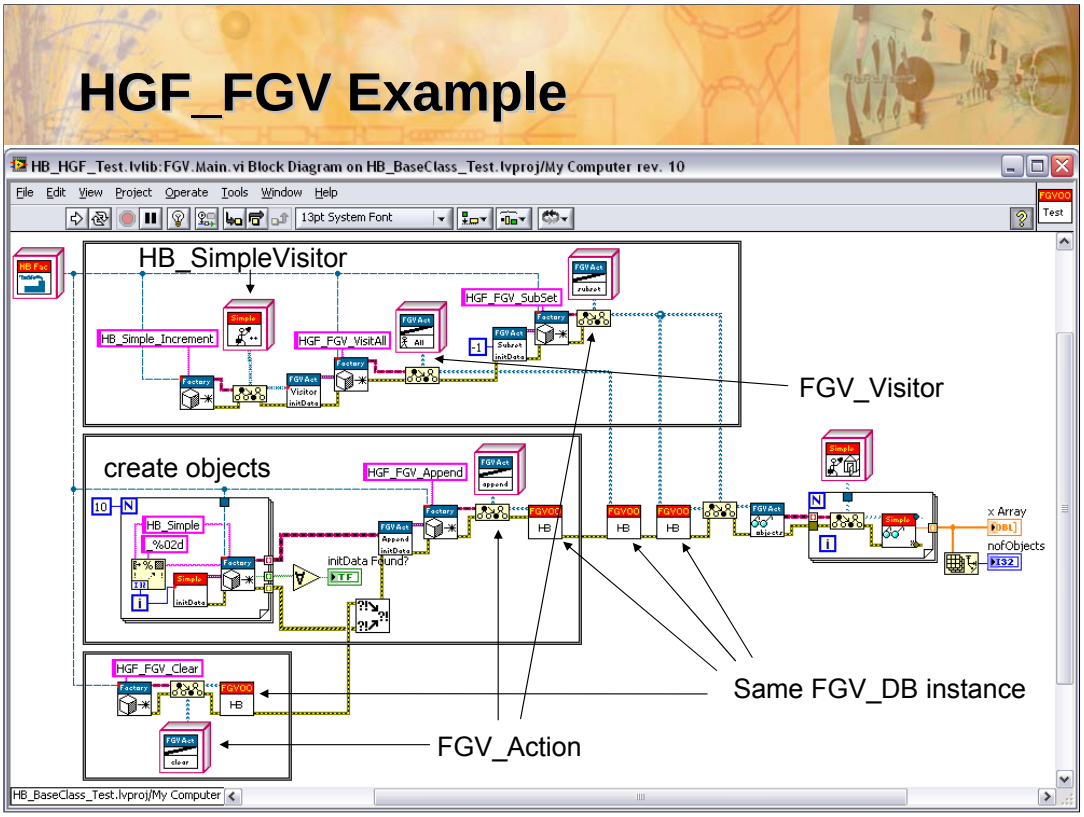
LabVIEW Objects are stored as array in a Functional Global Variable (uninitialized shift-register). The Visitor, an object inherited from *HGF_FGV_Action*, overrides the *action.vi*, to access or manipulate the *LabVIEW Objects stored in the FGV*, e.g. to append more object to the object array stored in the FGV. The *HGF_FGV.lvlib:FGV_DB.vi* is reentrant. A developer can make copies of the template *HGF_FGV.lvlib:FGV_DB.vit* to create different FGV_DB instances.



Two kinds of *HGF_FGV_Action* classes are available.

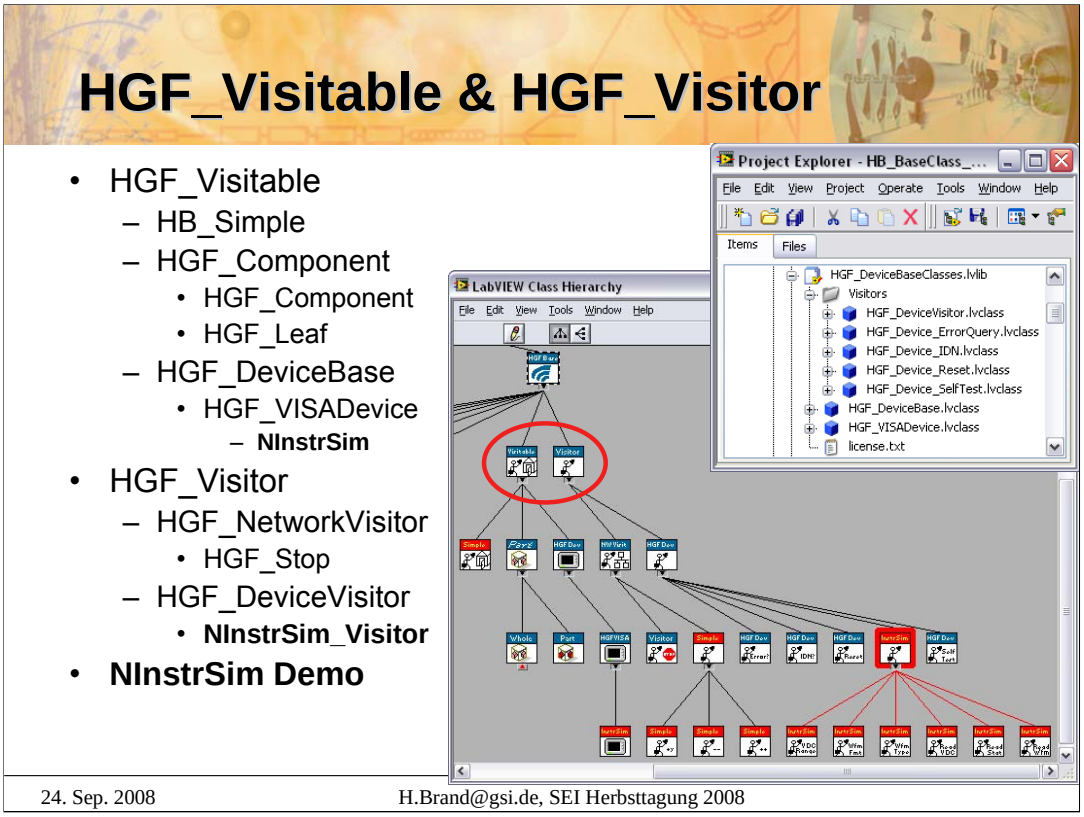
•Classes to manipulate the object array

•Classes to manipulate the objects stored in the object array
The *HGF_FGV_Visitor* carries the object *visitor* which knows what to do with the selected object.

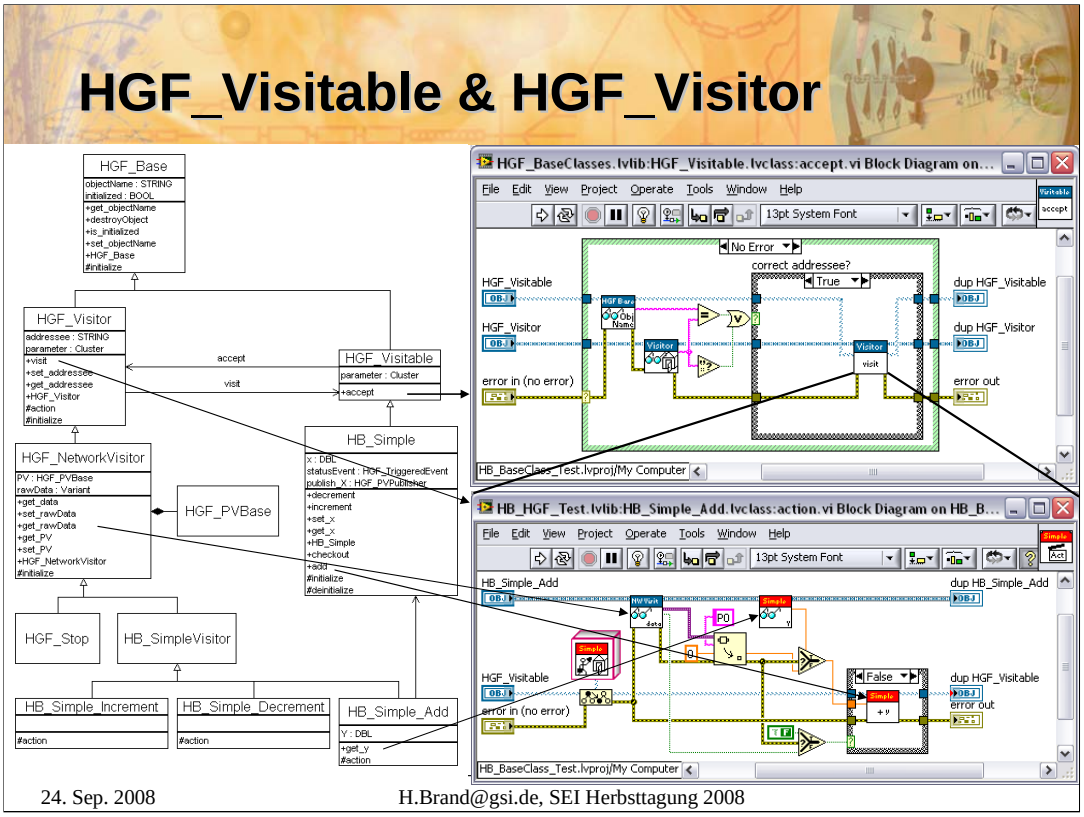


This example shows how to use *HGF_FGV_Action* and *HGF_FGV_Visitor* to manipulate objects that are stored in a FGV database instance.

The FGV DB instance is cleared in the very beginning. Then ten objects of *HB_Simple* class are created and appended to the FGV DB instance. Next a *HB_Simple_Increment* visitor, increments the object's attribute value x, is send to all object stored in the FGV_DB instance. Finally copies of all FGV_DB instance objects are requested to display their current values on the frontpanel.



The *HGF_FGV* has its own associates visitors. All other classes that use this design pattern inherit from *HGF_Visitable* which accept *HGF_Visitors*. Refer to next transparancy for more detSails.



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A UML digram of the Visitor pattern is shown on the left hand side, the blockdiagram of the relevant class methods on the right hand side.

Accept and **visit** are the names of the associations between the *HGF_Visitor* and *HGF_Visitable* classes.

If the *HGF_Visitor* object is accepted by a *HGF_Visitable*, it calls the visit method of the visitor. The visitor knows what to do and necessary parameters, the visitable knows how to do it.

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- **Questions? Comments?**
- **Starting Points for your own work**
  - http://wiki.gsi.de/cgi-bin/view/NIUser/LabVIEWObjectOrientedProgramming
  - http://wiki.gsi.de/cgi-bin/view/NIUser/HGFBaseClassLibrary
- **LVOOP Workshop**
  - http://wiki.gsi.de/cgi-bin/view/NIUser/LVOOPWorkshopMarch2007

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The next transparencies will introduce generic thread handling using LabVIEW classes. The corresponding design pattern is called **Thread Pool**.

Agents with Dataflow Objects?

- Separation of
  - **active generic threads**, that perform
  - **tasks**, that know **when** and **what** to do with
  - **passive objects** that provide the functionality.
    The object knows how operate on its attribute data.
  - Idea → Thread Pool
    - Thread Manager → HGF_ThreadPool
    - Worker → HGF_ThreadWorker
    - Tasks → HGF_ThreadTask
  - Events & Exceptions
- Diploma thesis about LabVIEW Agents
  - started this week at GSI → Frederik Berck.

GSI

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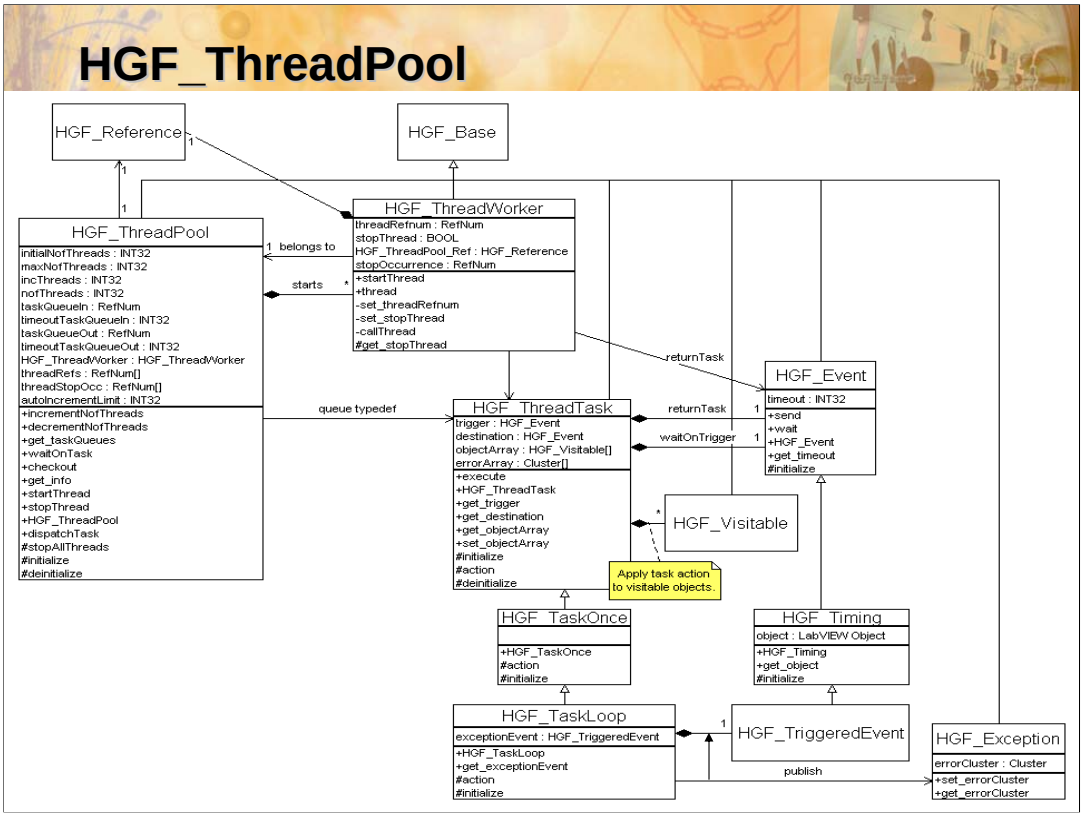
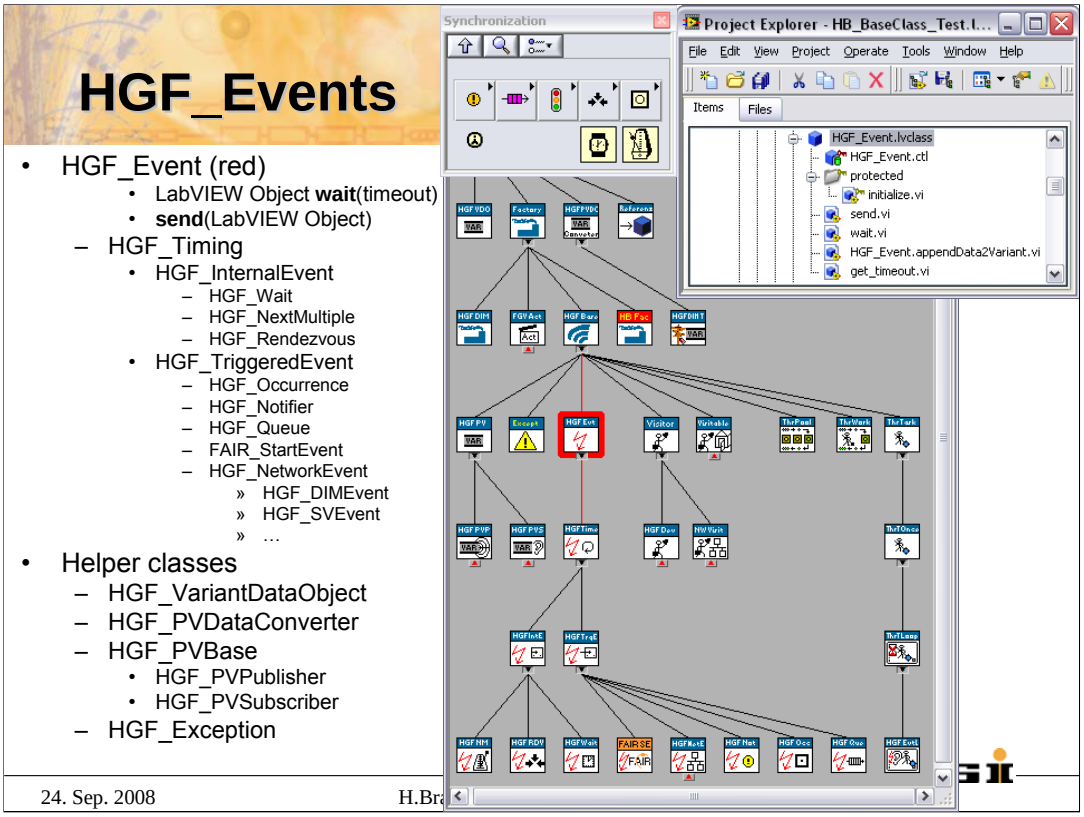
LabVIEW classes provide private data and member VIs operating on that data only. Though all LabVIEW class a passive and in a way extended wire types only. But similar to the *BaseProcess* class within the *CS* Framework or active classes in Java, it would be nice have active objects within LabVIEW that perform (quasi-) periodic actions or react on external and internal events in a distributed computing environment. The corresponding design pattern is called **Agent**. An Java Agent Development System has been introduced already before 1999, Aglets in CERN Summer School of Computing (book reference to be inserted here).

In LabVIEW the driving program or active threads, **Worker** started and maintained by a **ThreadPool**, have to be separated from **Tasks**, that know what to do with passive data objects. The problem should be solved very generic to enforce reusability and avoid code duplication. That leads to the ***HGF_ThreadPool*** design pattern as well as **Event** and **Exception** classes.

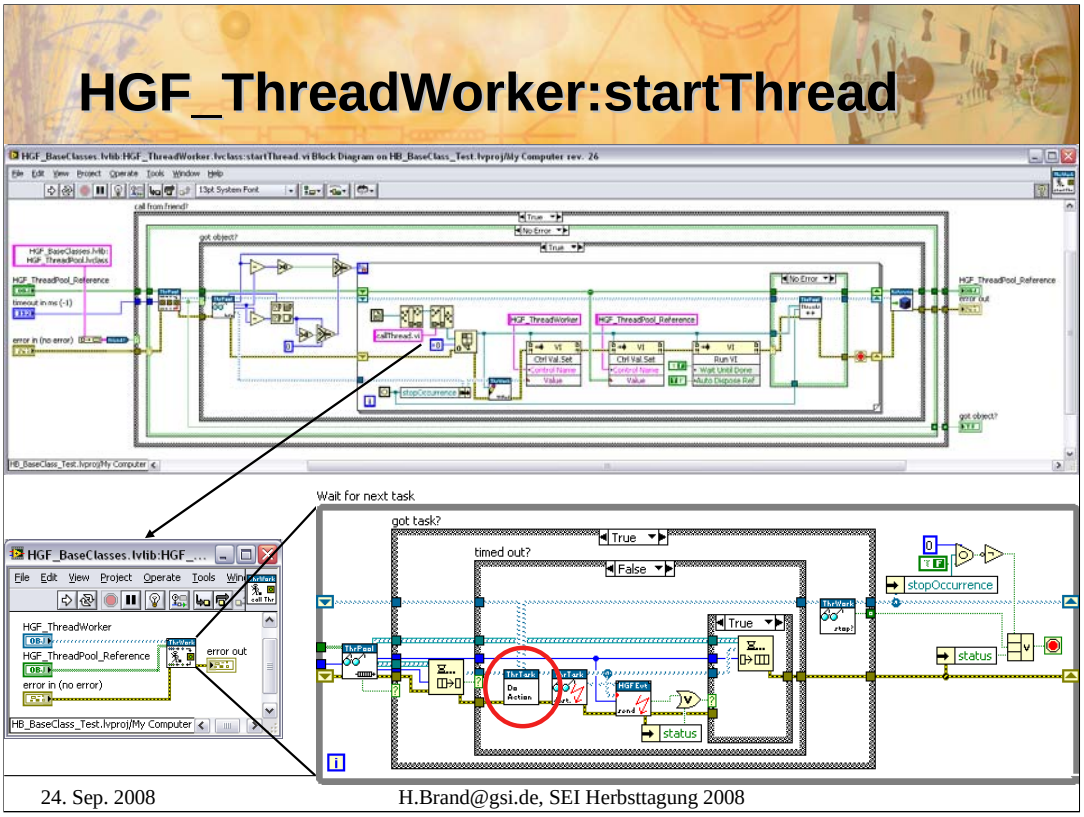


This transparency shows the UML class diagram of the Thread Pool. Objects of *HGF_ThreadPool* must be entities, stored in *HGF_Reference* objects, since they start and maintain active threads, *HGF_ThreadWorker*. The *HGF_ThreadWorker* performs the actions defined by the *HGF_ThreadTask*. *HGF_ThreadWorker* and *HGF_ThreadTask* are base classes. Child classes can override the default implementation of *HGF_ThreadWorker.lvclass:thread.vi* and *HGF_ThreadTask.lvclass:action.vi* methods.

A *HGF_ThreadWorker* takes the next *HGF_ThreadTask* from the input queue of *HGF_ThreadPool* and executes its *action.vi* and send it to the desired destination, a *HGF_Event*, or the default task output queue of *HGF_ThreadPool*. *HGF_ThreadTask.lvclass:action.vi* contains the implementation of the task to be executed, that means the task knows what to do. *HGF_ThreadTask* provides an visitable object array in its attribute that could be used by any child class. A *HGF_ThreadTask* may wait for a (visitor received from an) trigger event before performing the (visitors) action. *HGF_TaskOnce* and *HGF_TaskLoop* are child classes of *HGF_ThreadTask*. *HGF_TaskOnce* performs a visitors action once on all visitable objects and returns with the results. *HGF_TaskLoop* waits in a while loop for arriving visitors to perform their actions. Since the task typically does not return, he has to send the visitor to his desired destination. HGF_Exceptions are published via *HGF_TriggeredEvent*s.

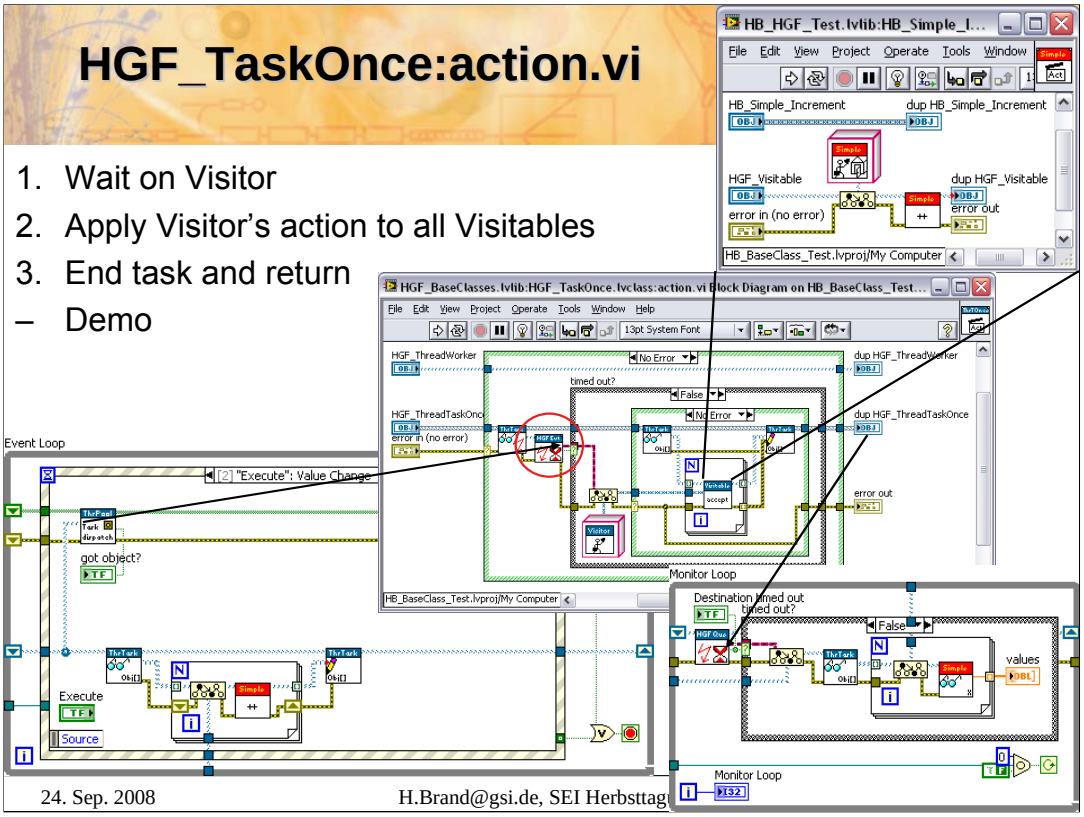


This transparency shows the *HGF_Event* class hierarchy. *HGF_Event* is marked with a red square. Most LabVIEW event sources are implemented as child class of *HGF_Event*. There are internal event like Wait, WaitOnNextMultiple, Rendezvous. Other events can be triggered, e.g. Occurrence, Notifier, Queue, or Network events, e.g. Shared Variable or DIM. Network event require some helper classes to enable generic programming dealing with process variables (PV). HGF_Exception could maybe used to extend LabVIEWs concept of error handling. (*FAIR_StartEvent* is a joke, for insiders only!)



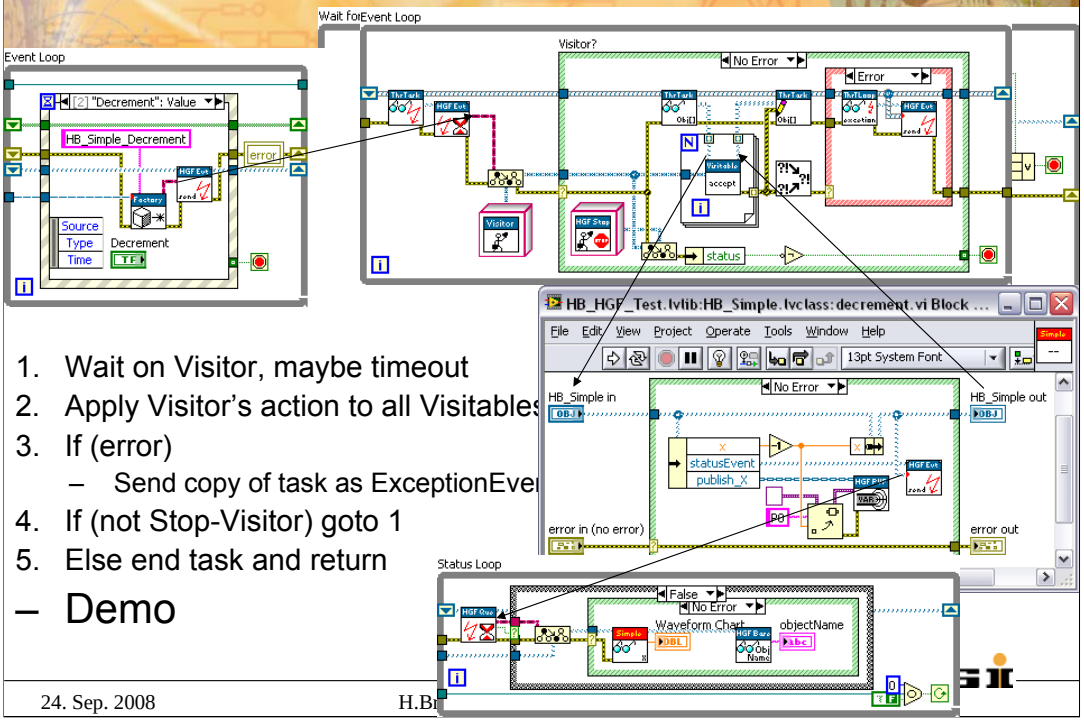
LabVIEW make thread handling very easy. Just draw loops with no data dependency on the block diagram and they will become executed in parallel. But this aproach requires explicit programming and wiring. A more generic approach like a Thread Pool make things slightly complicate. One has to use VI-Server methods and properties to start asynchronous threads programmatically. One also has to deal with the VI references and has to cleanup carefully. The upper blockdiagram shows how threads are started within the *HGF_ThreadPool*. (For technical reason this VI has to be member of HGF_ThreadWorker. The user will call *HGF_ThreadPool.lvclass:startThread.vi* which internaly calls *HGF_ThreadWorker.lvclass:startThread.vi*)

HGF_ThreadWorker.lvclass:callThread.vi is reentrant and call the dynamic dispatch method *HGF_ThreadWorker.lvclass:thread.vi*, which is partly shown in the lower right corner. The red circle marks the public *HGF_ThreadTask.lvclass:execute.vi* performing the real protected dynamic dispatch VI *HGF_ThreadTask.lvclass:action.vi* which can be overwritten by childclasses.



This example shows how a *HGF_TaskOnce* object, containing a visitable object array, is dispatched from the Event Loop of main.vi to a *HGF_ThreadPool*. *HGF_TaskOnce* waits for the Visitor, which is in this example a parameter of the *HGF_Event*. *HGF_TaskOnce* then applies the visitors action to all visitable objects, in this example it is incrementing the attribute X of *HB_Simple* class. Next *HGF_TaskOnce* is send to its desired destination and received in the Monitor Loop of the main.vi. Here the *HGF_TaskOnce* object is asked for the result of its action.

HGF_TaskLoop:action.vi



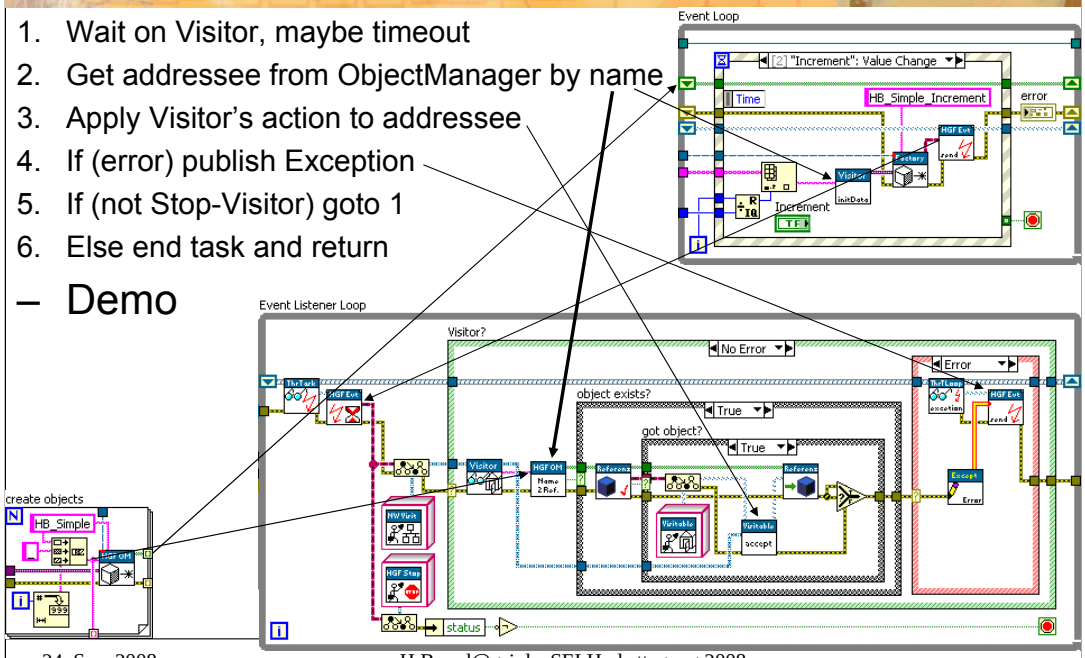
1. Wait on Visitor, maybe timeout
2. Apply Visitor's action to all Visitables
3. If (error)
   - Send copy of task as ExceptionEve
4. If (not Stop-Visitor) goto 1
5. Else end task and return

– Demo

HGF_TaskEventListener:action

1. Wait on Visitor, maybe timeout
2. Get addressee from ObjectManager by name
3. Apply Visitor's action to addressee
4. If (error) publish Exception
5. If (not Stop-Visitor) goto 1
6. Else end task and return

– Demo



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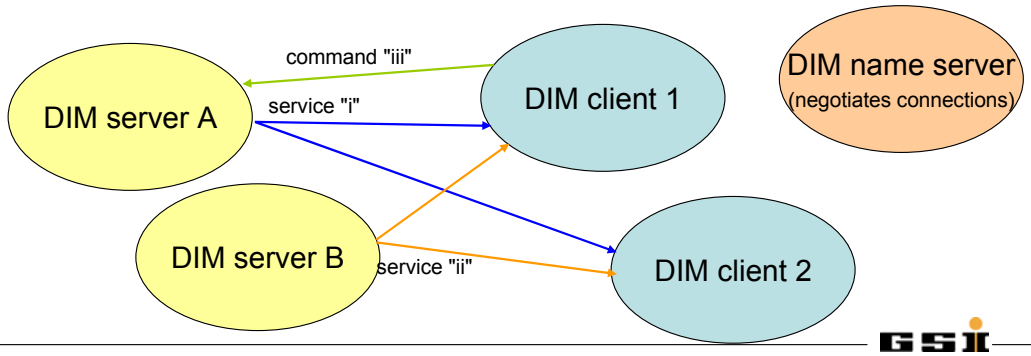
The first part of the talk will introduce LabVIEW, discuss the usage of object oriented software design and points out the difference to conventional object oriented programming languages.

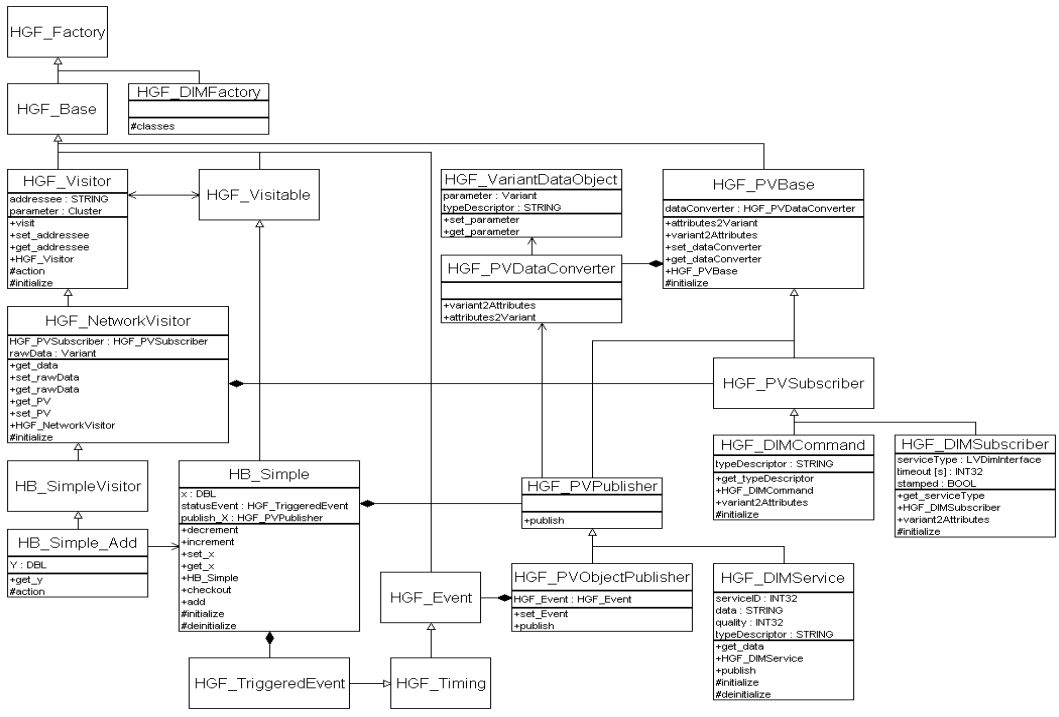
The second part of the talk will focus on LVOOP Design Patterns that enables the usage of LabVIEW objects as entities. The HGF Base Class library contains an implementation of important design patterns with respect to the dataflow paradigm.

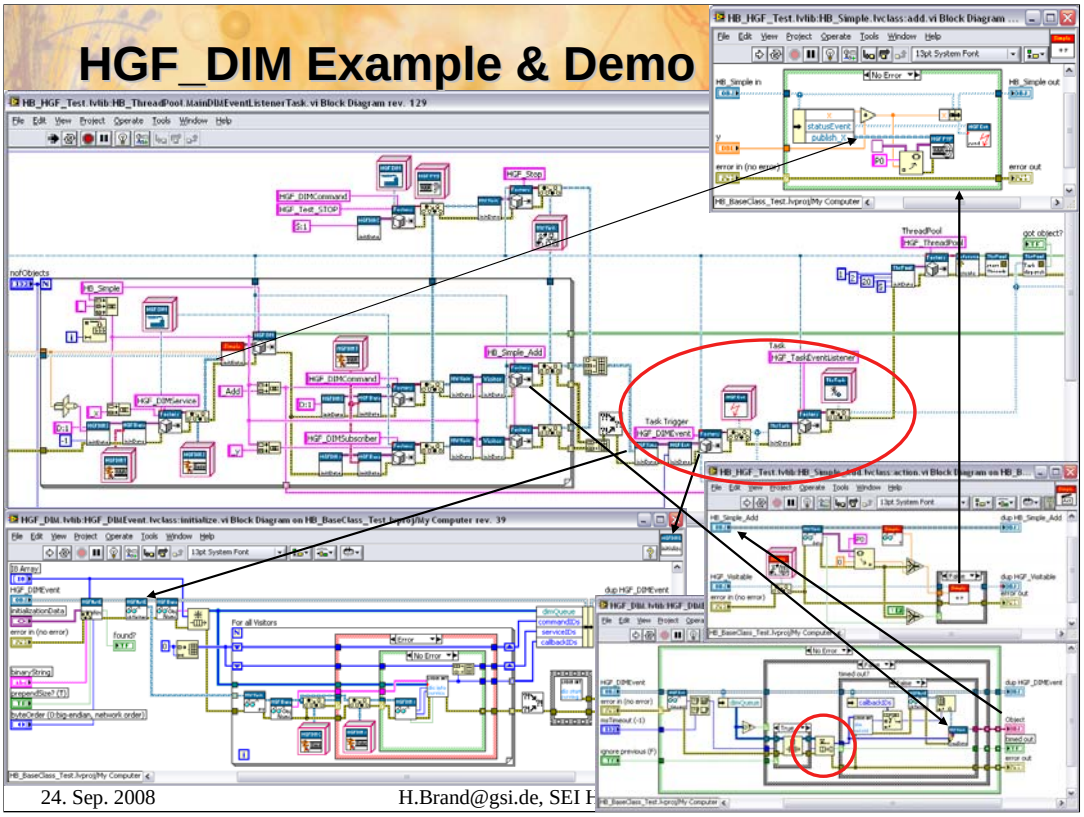
Communication Layer: DIM

- Distributed Information Management: www.cern.ch/dim
- originally developed at DELPHI@LEP/CERN around 1991
- available for a multitude of platforms and languages
- light-weight, aiming at high performance, based on TCP/IP
- today: "backbone" of control systems for LHC experiments
- concept: named services, peer-to-peer connections



ProcessVariable & DataConverter





Thank for your attention!

- Questions?
- Starting Points for your own work
  - http://wiki.gsi.de/cgi-bin/view/NIUser/LabVIEWObjectOrientedProgramming
  - http://wiki.gsi.de/cgi-bin/view/NIUser/HGFBaseClassLibrary
- LVOOP Workshop
  - http://wiki.gsi.de/cgi-bin/view/NIUser/LVOOPWorkshopMarch2007

HELMHOLTZ ZENTRUM BERLIN
für Materialien und Energie

Hochpräzise Messung transienter Oberflächenphotospannungen

S. P. Bönisch, Th. Dittrich, S. Dube, P. Zabel

**SEI-Tagung, Max-Planck-Institut für Plasmaphysik,
IPP-Teilinstitut Greifswald, 22.- 24.9. 2008**

HELMHOLTZ ZENTRUM BERLIN
für Materialien und Energie

Inhalt

- Einleitung
- Meßprinzip
- Meßaufbau
- Meßdatenaufbereitung
- Ergebnisse
- Zusammenfassung

Motivation

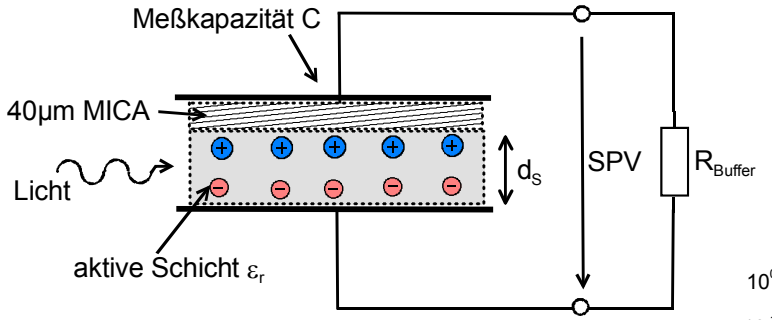
Untersuchung von Ladungsträgergenerations- und Relaxationsmechanismen an Modellsystemen photoaktiver Materialien bzw. Materialsystemen mit Schichtdicken im molekularen Bereich (nm).

Messung der transienten Oberflächenphotospannung mit:

1. ≥10GΩ Eingangsimpedanz
2. ≤10µV Auflösung
3. 8 Größenordnungen im Zeitbereich
4. In extrem störbehafteter Umgebung
5. Logarithmisch zeitskalierter Ausgabe

Einbindung in bereits bestehende Aufbauten, sowie möglichst variable Anwendbarkeit im Labor ist eine weitere Herausforderung für diese Entwicklung!

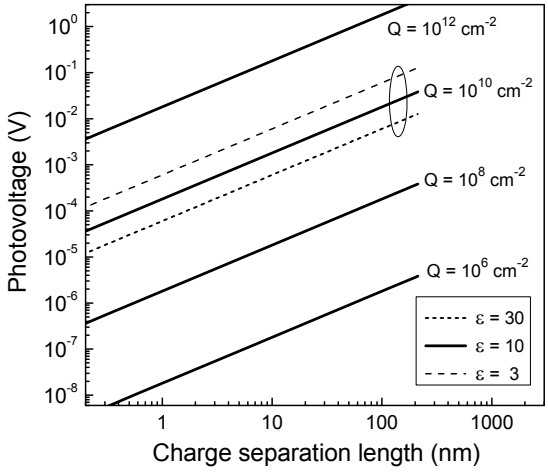
Oberflächenphotospannung



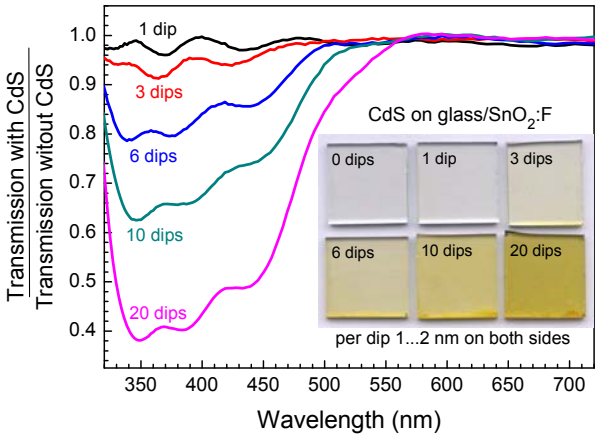
Oberflächenphotospannung:
surface photo voltage (SPV)

$$SPV = Q \cdot \frac{1}{\varepsilon \cdot \varepsilon_0} \cdot d_S$$

- Separierung von Ladungsträgern
- Auskopplung über Influenz
- Begrenzung der zeitlichen Auflösung durch Bandbreite des Meßsystems und Zeitkonstante C^*R_{Buffer}



Probenpräparation Modellsystem



Konzentration von absobierten Photonen:
Concentration of absobed photons (C_{ph})

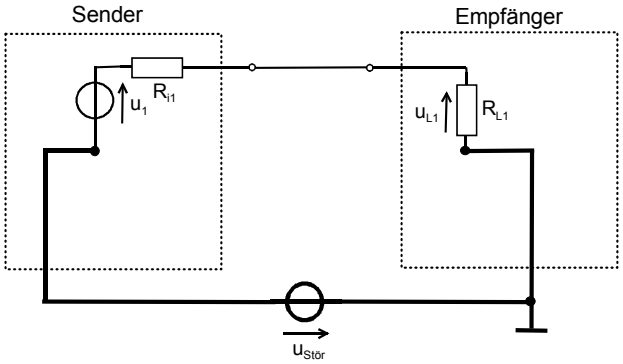
$$C_{ph} = \frac{I}{\hbar\omega \cdot q} \cdot \left(1 - \exp(-\alpha \cdot d_S)\right)$$

I – Intensität [J/cm²]
q – Elementarladung (1.6*10^{-19} C)
ħω – Bandlücke (3.7eV)
α – Absorptionskoeffizient (Abbildung)
d_s – Separationslänge (≈Schichtdicke)

- Photoaktive Schicht CdS, 1-40nm auf SnO_2 Glas
- Beschichtung mittels ILGAR-Verfahren (ion layer gas reduction)
- Tauchen in $Cd(ClO_4)_2$-Lösung, Diffusion von H_2S bei 160°C
- 1xTauchen = 1dip = 2nm

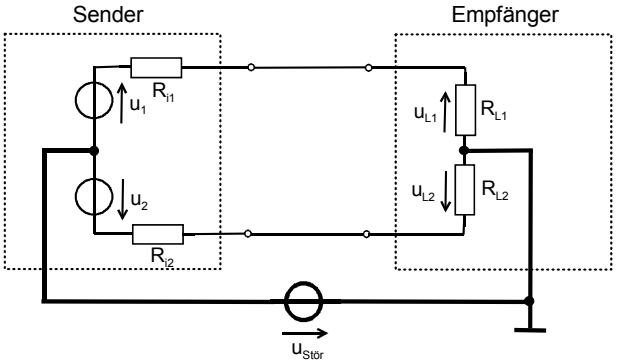
Meßprinzip

Single-Ended (unsymmetrisch)



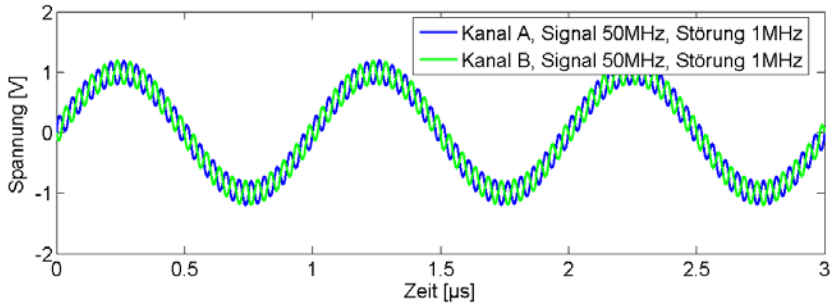
+einfacher Aufbau
-Empfindlich gegen Gleichtaktstörungen

Differentiell (symmetrisch)

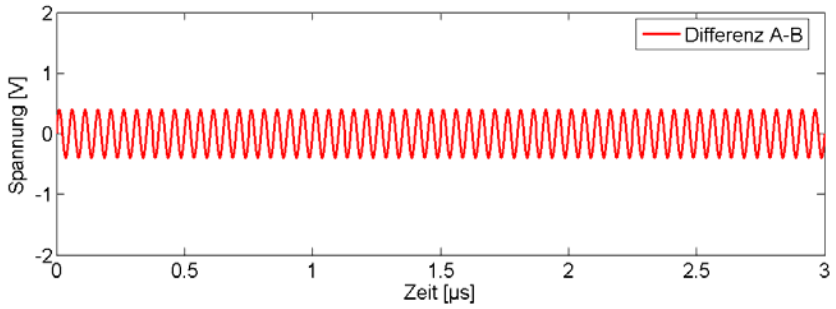


komplizierter Aufbau
Störunempfindlich!
(ca. 40dB besserer Signal-Störabstand)

Störunterdrückung durch Differenzbildung

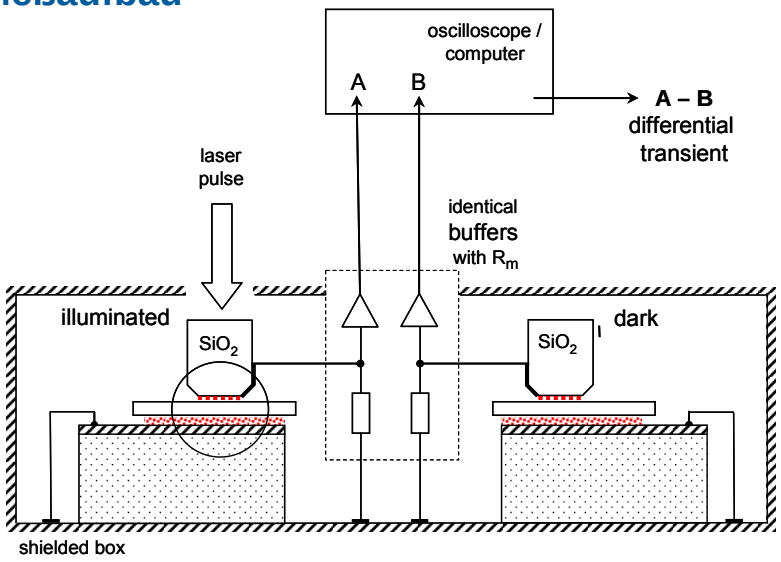


Differentielle Signale mit überlagerter Gleichtaktstörung



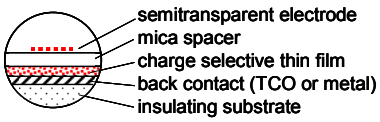
Gleichtaktstörung wird durch Differenzbildung eliminiert

Meßaufbau

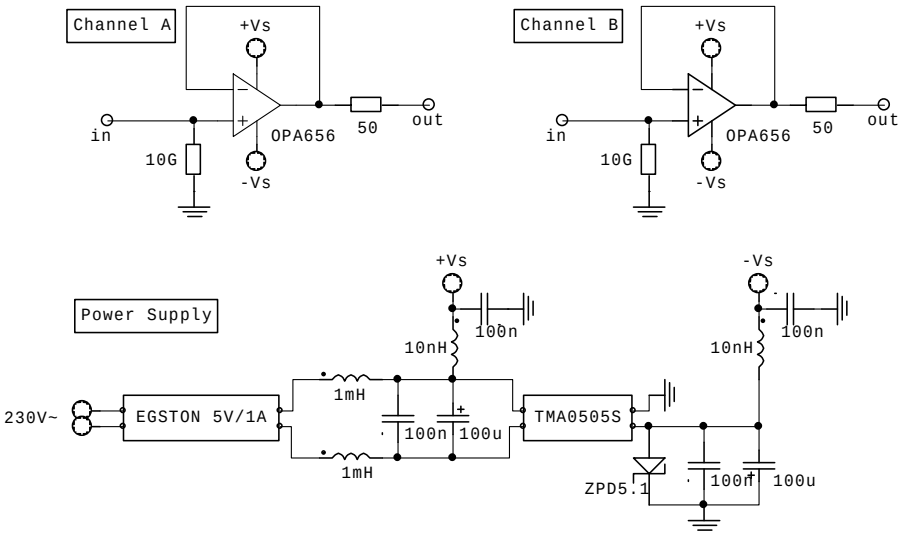


Spezifikationen:
- Differentielles Meßprinzip
- Logarithmisch zeitskalierte Auslese
- Gleitende Mittelung
- Meßzeit ≤ 1s
- Probenkapazität ≤ 100pF
- Bandbreite ≥100MHz
- Digitalisierung 14bit, 100MS/s, 10^8 Samples

identical measurement capacitors

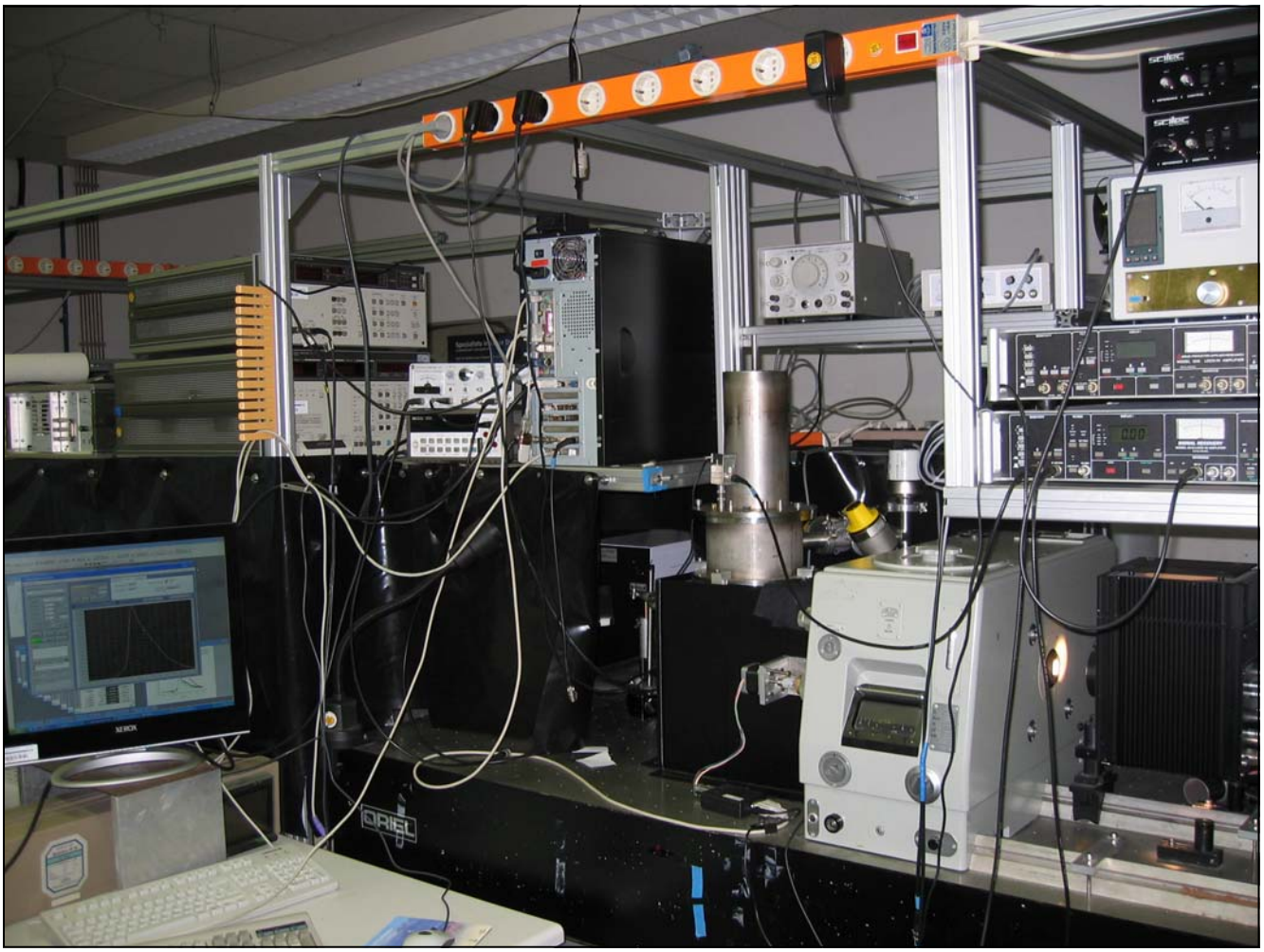


Schaltung



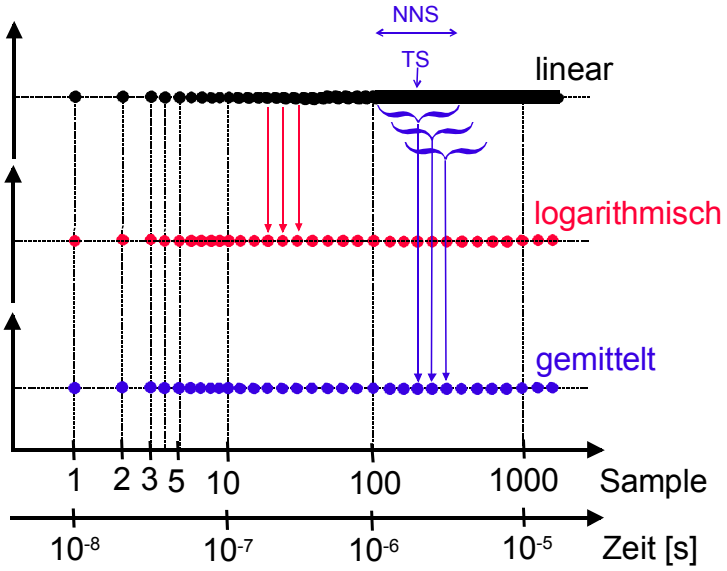
- Eingangswiderstand frei wählbar
- Schaltnetzteile und Filterung zur Störunterdrückung

Spezifikation:
- Eingangsimpedanz 10GΩ || <1pF
- Verstärkung = 1
- DC-Offset ≤ 1mV
- Rauschen ≤ 7nV/√Hz
- Bandbreite > 500MHz



Datenaufbereitung

- Datenreduktion durch logarithmischen Sampleabstand
- Gleitende logarithmische Mittelung

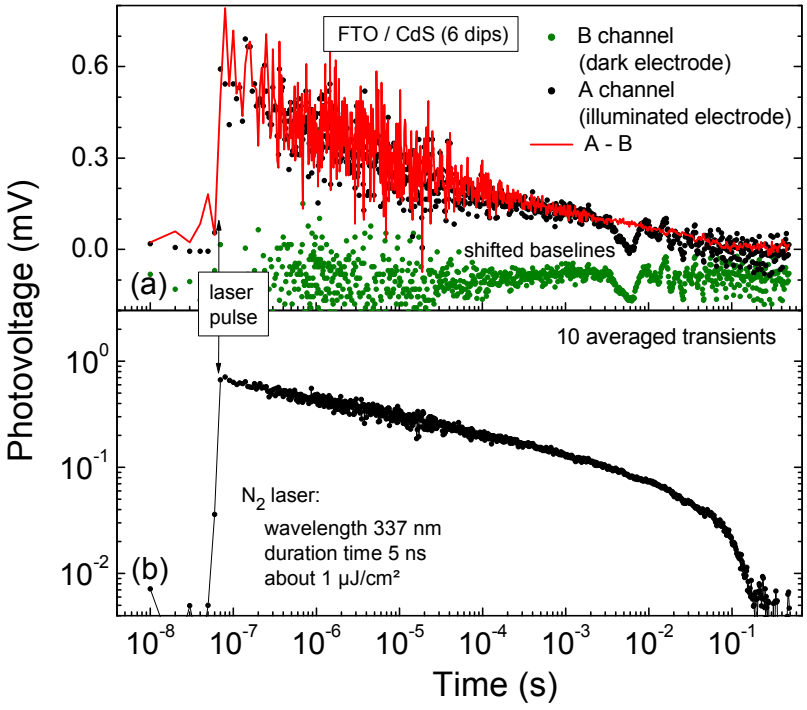


Anzahl von Datenpunkten für gleitende Mittelung:

$$NNS = \mathrm{int}\left(\frac{10\cdot\exp\left(\frac{TS}{60}\right)+48}{1000}\right)$$

NSS - number of neighboured samples
TS - time sample

Ergebnisse – Meßsystem

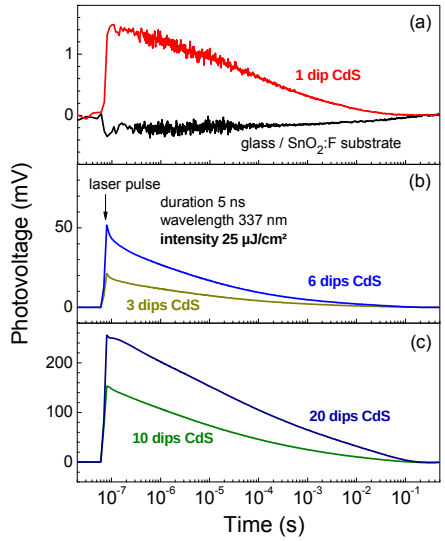


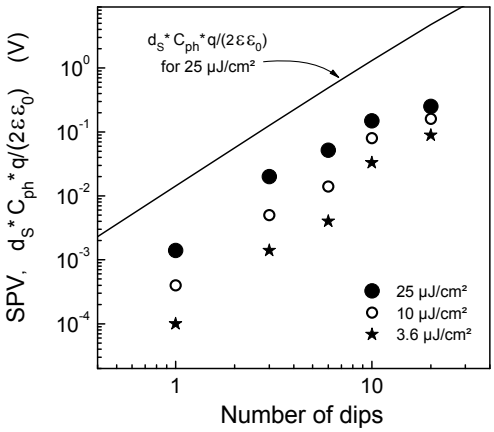
a) Direkte Messung Kanal A & B:
- Hochfrequente Störungen und Rauschen ≈200µV
- 50Hz Störungen ≈100µV

Differenz A-B:
- Hochfrequente Störungen ca. Faktor √2 größer (unkorreliert)
- 50Hz Störungen A-B ≈20-30µV

b) Mittelung über 10 Messungen:
- 50Hz Störungen ≈10µV (weitere Verbesserung mit √N)

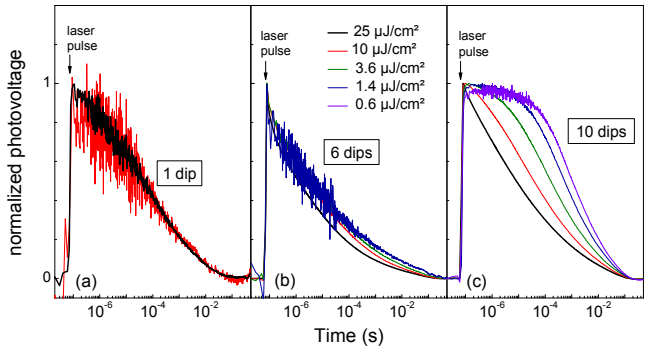
Ergebnisse – Ladungsträgergeneration

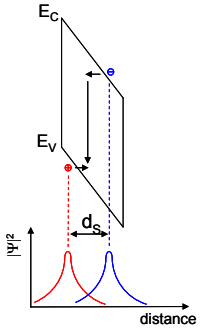




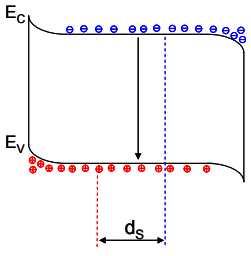
- Gemessene Oberflächenphotospannungen ca. Faktor 10 kleiner als theoretisches Maximum ($Q=C_{ph}$)
- Oberflächenphotospannung steigt mit CdS-Schichtdicke
- Sättigungseffekt bei großen Ladungsträgerdichten durch Rekombination ($Q\approx10^{13}$ cm^{-2})
- Unverstandener Effekt bei Schichtdicken >20nm (>10dips)

Ergebnisse – Relaxationsmechanismus





(a) tunneling controlled recombination



(b) diffusion controlled recombination

a) 2nm Schichtdicke (1dip):
Kurvenform unabhängig von Intensität
-> Tunneleffekt-kontrollierte Rekombination

b) 12nm Schichtdicke (6dips):
Übergangsbereich

c) 20nm Schichtdicke (10dips):
Kurvenform fällt schneller mit zunehmender Intensität
-> Diffusions-kontrollierte Rekombination (hohe Rekombinationsrate bei hoher Ladungsträgerkonzentration)

Zusammenfassung

•Meßsystem ermöglicht hochpräzise Messung transienter Oberflächenphotospannungen
•Oberflächenphotospannung steigt mit der Schichtdicke einer photoaktiven CdS-Schicht
•Sättigungseffekt bei hohen Ladungsträgerkonzentrationen infolge Rekombination
•Relaxationsmechanismus verändert sich bei einer CdS-Schichtdicke von ca. 12nm
•Verfahren sehr gut geeignet für Untersuchungen der Ladungsträgergeneration in molekularen Strukturen

Hochpräzise Messung transienter Oberflächenphotospannungen

HELMHOLTZ ZENTRUM BERLIN für Materialien und Energie

Herzlichen Dank an alle am Projekt beteiligten Personen:

•Projektleitung Dr. Thomas Dittrich / SE2
•Hardware Dr. Sven Bönisch / WTE
•Software Sascha Dube / WTE
•Auswertung Meßdaten Philipp Zabel / SE2
•Probenpräparation H. Muffler

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High precision differential measurement of surface photovoltage transients on ultra-thin CdS layers

Th. Dittrich, S. Bönisch, P. Zabel, S. Dube

High-impedance buffer and set-up for differential transient SPV measurements

The electric part of the measurement system consisted of 2 identical single ended high impedance buffer amplifiers with 50 Ω output. Both output signals were digitized using a 2-channel DAQ-Board (CompuScope 14200, GAGE, bandwidth 100 MHz, resolution 14 bit, used sampling rate 100 MS/s, 10^8 samples). The buffer amplifiers were standard industry grade JFET-input OPAMP's from Texas Instruments OPA656, configured as unity-gain voltage followers. The input impedance was given by the input shunt resistance of 10 GΩ. Special attention had to be paid to the power supply. Shielded switch mode power supplies and extensive filtering were used for optimum rejection of main disturbance. The electrical specifications of the buffer amplifiers were: input impedance 10 GΩ, < 1 pF; output voltage swing ± 2 V; gain 0 dB, non-inverting; DC-offset < 1 mV; bandwidth 500 MHz; input noise voltage density 7nV/$Hz^{0.5}$ (f > 100 kHz); power supply +-5 V DC, 100 mA.

The heart of the set-up consisted of the two identical measurement capacitors connected with the two identical high impedance buffers. The measurement capacitors were formed by the back contact of the sample, an ultra-thin charge selective layer, a mica spacer (about 40 µm thick) and a quartz cylinder with a transparent SnO_2:F electrode. The SnO_2:F electrodes were gently pressed on the mica spacers via a cardanic spring. One electrode remained in the dark whereas the other electrode was illuminated with laser pulses (N_2 laser, pulse duration time 5 ns, wavelength 337 nm, repetition rate 1 Hz, intensity between 0.6 and 25 µJ/cm²). As remark, there is no principal need for two identical electrode configurations since a circuit identical to the illuminated electrode with the sample would be sufficient for the differential SPV measurement. But it was much easier to realize two identical electrode configurations in our experiments.

The two outputs of the high-impedance buffers were connected with the two channels (A and B) of the oscilloscope. For triggering with a jitter less than 1 ns a part of the light pulse was reflected with a beam splitter to a Si photodiode with an amplifier. The signal of the photodiode was transformed to a TTL-trigger pulse in the sensitive amplifier. Common mode disturbance gave identical signals on channels A and B since the measurement capacitors and the high-impedance buffers were identical. Therefore, common mode disturbance disappeared in the differential transients A – B. The differential transient was formed by software in the personal computer.

Logarithmic read-out of one transient over 8 decades and averaging

The huge amount of 10^8 data points per transient is measured on board of the DAQ. The full read-out of each transient would demand tremendous resources for experiments in time and memory in the computer. However, most of the data points do not carry useful information in SPV experiments since processes change usually logarithmically. Therefore, the read-out of data points was reduced from a linear time scale to equidistant samples in a logarithmic time scale. The number of registered data points per transient was reduced from 10^8 to less than 10^3 by introducing a special read-out and averaging algorithm. Due to this measure, first, the transfer rate of transients from the DAQ to the computer increased by about 3 orders of

magnitude, second, the statistic noise rejection improved at longer times depending on an averaging parameter (K_A), and, third, the memory needed for one stored transient decreased by 5 orders of magnitude.

The time values in the transients one would like to safe on the computer were numbered by 1, 2, 3 … ~1000 ($P_{read\text{-}out}$). The values of $P_{read\text{-}out}$ have to be set into a relation to the numbers of the selected time values in the memory of the DAQ ($P_{on\text{-}board}$). The values of $P_{read\text{-}out}$ and $P_{on\text{-}board}$ were equal for the first 100 data points in the transients. The trigger was set after the first 6 samples to fix the base line. Starting with $P_{read\text{-}out}$ = 101, the values of $P_{on\text{-}board}$ were selected by using the following empirical equation

$$P_{on-board} = \mathrm{int}\left(10 \cdot \exp\left(P_{read-out}/60\right)\right) + 48 \qquad (1)$$

The exponential increase in equation (2) was chosen in such a way that the remaining 6 orders of magnitude in time were covered by 800…900 values of $P_{on\text{-}board}$.

Additionally, a procedure has been implemented for $P_{read\text{-}out}$ > 100 in order to decrease the noise by averaging over neighboured samples. With respect to equation (1) the number of neighboured samples (NNS) at a certain value of $P_{read\text{-}out}$ increased also exponentially

$$NNS = \frac{\mathrm{int}\left(10 \cdot \exp\left(P_{read-out}/60\right)\right) + 48}{K_A} \qquad (3)$$

The product of the time and of the inverse of the parameter K_A at a given value of $P_{read\text{-}out}$ can be understood as an exponentially increasing integration time constant in a transient measurement. For the given experiments, K_A was set to 1000.

The measured transients were subtracted to attain a differential measurement. The applied measures facilitated an exceedingly high suppression of interference or correlated potential fluctuations of more than 40 dB compared to a single ended measurement system.

Summary

Time-resolved surface photovoltage (SPV) is an important method for studying charge separation, for example, in nano-structured semiconductors. High precision differential measurement of SPV transients was realized with two identical measurement capacitors and high-impedance buffers. In addition, logarithmic read-out and averaging procedures were implemented for single transients over 8 magnitudes in time. As a model system ultra-thin CdS layers were investigated. The thickness dependencies of the SPV amplitudes and that of the dominating relaxation mechanisms are demonstrated and discussed.